

» User Guide «

AM4100

**Single Mid- and Full-Size AMC Module
based on the Freescale™ MPC8641D
Dual-Core PowerPC® Processor**

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Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

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Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.



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Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

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Caution, Electric Shock!

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Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.



Warning!

This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.



It is particularly important to observe standard anti-static precautions when changing piggy-backs, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.



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Kontron grants the original purchaser of Kontron's products a **TWO YEAR LIMITED HARDWARE WARRANTY** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

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Chapter

1

Introduction



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1. Introduction

1.1 Board Overview

The AM4100 is a highly integrated CPU board implemented as a Single Mid-size or Full-size Advanced Mezzanine Card (AMC) Module. The design is based on the Freescale™ MPC8641D dual-core PowerPC® processor, which uses two e600 cores and high-speed interconnect technology to balance processor performance with I/O system throughput for networking, storage, wireless infrastructure and general-purpose embedded applications.

The MPC8641D is a highly integrated system-on-chip (SOC) platform that consists of two e600 cores each having 32 kB L1 instruction cache, 32 kB L1 data cache and 1 MB L2 cache, a high-speed DDR2 memory interface, four triple speed Ethernet controllers (TSECs), a x4 Serial RapidIO™ fabric interface, a x4 PCI Express I/O interface and a high-performance MPX bus that scales to 600 MHz.

The board is capable of supporting core frequencies ranging from 1.0 GHz to 1.5 GHz providing up to 600 MHz platform speed. The processor and the memory are soldered on the AM4100 which results in higher Mean Time Between Failures (MTBF) and a significant improvement in cooling.

The AM4100 includes up to 2 GB unbuffered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running at frequencies up to 600 MHz. The four integrated TSECs ensure maximum data throughput between the processor and the Ethernet infrastructure. The board further provides up to 4 GB Flash memory via an onboard NAND Flash Controller.

The AM4100 has full hot swap capability, which enables the board to be replaced, monitored and controlled without having to shut down the ATCA carrier board or the MicroTCA system. A dedicated Module Management Controller (MMC) is used to manage the board and support a defined subset of Intelligent Platform Management Interface (IPMI) commands and PICMG (ATCA/AMC) command extensions, which enables operators to detect and eliminate faults faster at module level. This includes monitoring several onboard temperature conditions, board voltages and the power supply status, managing hot swap operations, rebooting the board, etc. All in all, IPMI enhances the board's availability and reliability while reducing the operating costs and the mean-time-to-repair.

As a "headless" AMC design (no onboard graphics controller), the AM4100 supports one standard RS232 serial port (SER0) and up to two Gigabit Ethernet ports on the front panel as well as a variety of high-speed interconnect topologies to the system, such as two Gigabit Ethernet SerDes connections in the Common Options Region, x4 PCI Express or Serial RapidIO connection and optional Gigabit Ethernet SerDes connection in the Fat Pipes Region, as well as a debug port and a serial port in the Extended Options Region.

Optimized for high-performance, packet-based telecom systems, the AM4100 is targeted towards, but not limited to the telecom market application such as radio network controllers, media streaming, traffic processing, database management and routing. The AM4100 also fits into all applications situated in industrial environments, including I/O intensive applications. The careful design and the selection of high temperature resistant components ensure a high product availability. This, together with a high level of scalability, reliability, and stability, make this state-of-the-art product a perfect core technology for long-life embedded applications.

The AM4100 is offered with various Board Support Packages. Please contact Kontron for further information concerning the operation of the AM4100 with other operating systems.



1.2 Board-Specific Information

Due to the outstanding features of the AM4100, such as superior processing power and flexible interconnect topologies, this AMC board provides a highly scalable solution not only for a wide range of telecom and data network applications, but also for several highly integrated industrial environment applications with solid mechanical interfacing.

Some of the AM4100's outstanding features are:

- Freescale MPC8641D processor, 1.0 GHz, 400 MHz platform frequency
- Freescale MPC8641D processor, 1.32 GHz, 528 MHz platform frequency
- Freescale MPC8641D processor, 1.5 GHz, 600 MHz platform frequency
- Up to 2 GB DDR2 SDRAM memory with ECC running at 400/528/600 MHz
- AMC interconnection
 - Two Gigabit SerDes connections in the Common Options Region
 - x4 PCI Express connection in the Fat Pipes Region (operates as a root complex controller) or alternatively x4 Serial RapidIO interface in the Fat Pipes Region (operates as host or as agent)
 - Two Gigabit SerDes connections in the Fat Pipes Region (optional)
 - Serial port in the Extended Options Region
 - Debug port in the Extended Options Region
 - PCI Express clock reference input, FCLKA
- Full hot swap support
- NAND Flash Controller for up to 4 GB memory
- One serial port on Front I/O (RS232)
- Two Gigabit Ethernet ports on Front I/O
- Two redundant NetBootLoader (NBL) Firmware Flash chips (2 x 4 MB)
- Dedicated IPMI Module Management Controller (MMC) with redundant MMC Firmware Flash
- Watchdog Timer
- JTAG interface for debugging and manufacturing purposes
- Four bicolor debug LEDs
- Standard temperature range: -5°C to + 55°C
- Passive heat sink solution (system air flow required)
- Single Mid-size and Full-size AMC module
- Designed to be compliant with the following specifications:
 - PICMG AMC.0, Advanced Mezzanine Card Specification R2.0
 - PICMG AMC.1, PCI Express and Advanced Switching R1.0
 - PICMG AMC.2, Gigabit Ethernet R1.0
 - PICMG AMC.4, Serial RapidIO (Draft 0.4)
 - PICMG MTCA.0 Micro Telecommunications Computing Architecture R1.0
 - IPMI - Intelligent Platform Management Interface Specification, v2.0, R1.0
- Kontron NetBootLoader



1.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the AM4100.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
Hardware Requirements	The AM4100 can be installed on any AMC-supporting carrier board or MicroTCA backplane with the following AMC Card-edge connector port mapping: • Common Options Region ports 0-1 • Two Gigabit Ethernet SerDes ports • Fat Pipes Region ports 4-7 • One x4 PCI Express interface, or alternatively • x4 Serial RapidIO interface • Fat Pipes Region ports 8-9 • Two Gigabit Ethernet SerDes ports (optional) • Extended Options Region port 14 • Reserved for debug port • Extended Options Region port 15 • One serial port • Clock • PCI Express clock reference input, FCLKA For further information on the AMC interconnection, refer to section 2.4, "AMC Interconnection".
PCI Express Configuration	The AM4100 supports PCI Express root complex configuration.
Operating Systems	The AM4100 is offered with various Board Support Packages. Please contact Kontron for further information concerning the operation of the AM4100 with other operating systems.

1.4 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

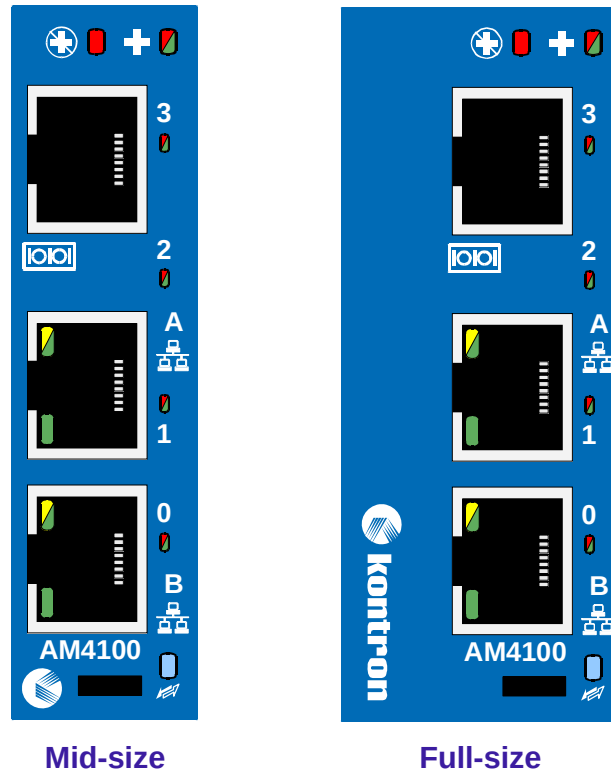
1.4.1 Functional Block Diagram

The following figure shows the block diagram of the AM4100.



1.4.2 Front Panel

Figure 1-2: AM4100 Front Panel Versions



Module Management LEDs

- | | | |
|--|---------------------------|---|
| | • LED1 (red): | Out-of-Service LED |
| | • LED2 (red/green/amber): | Health LED |
| | • HS LED (blue): | The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are <i>off</i> , <i>short blink</i> , <i>long blink</i> , and <i>on</i> . |

User-Specific LEDs

- | | | |
|--|----------------------------|---|
| | • ULED3 (red/green/amber): | AMC Eth. port A link signal status or POST code LED |
| | • ULED2 (red/green/amber): | AMC Eth. port B link signal status or POST code LED |
| | • ULED1 (red/green/amber): | Freely configurable or POST code LED |
| | • ULED0 (red/green/amber): | Freely configurable or POST code LED |

Connectors

- | | |
|--|------------------------------|
| | • Serial Connector |
| | • Gigabit Ethernet Connector |

For further information on the LEDs used on the AM4100, refer to section 2.3.1, “Front Panel LEDs”.



1.4.3 Board Layouts

Figure 1-3: AM4100 Board Layout (Top View)

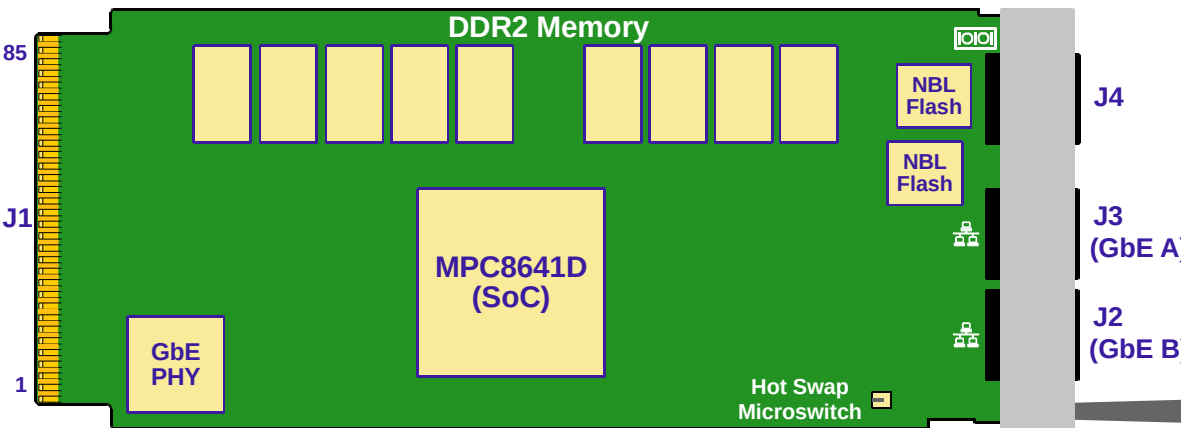
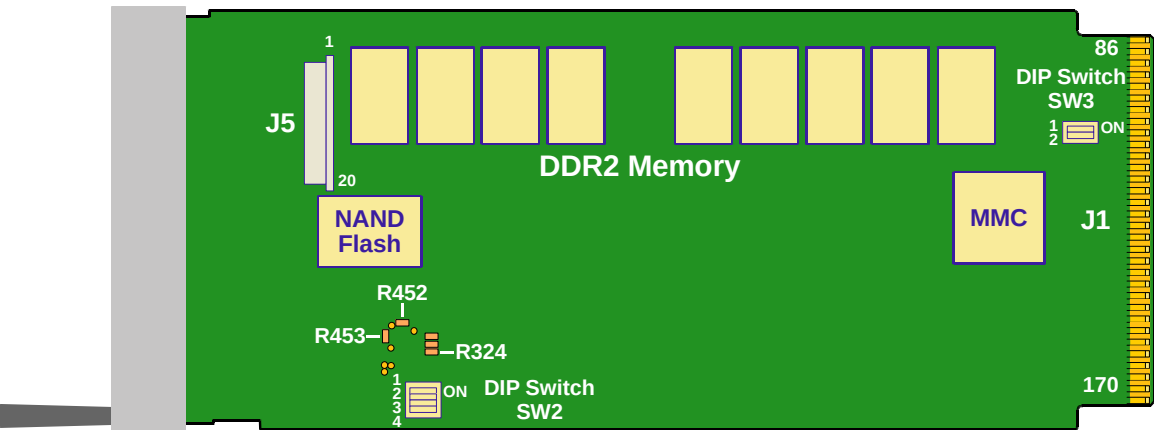


Figure 1-4: AM4100 Board Layout (Bottom View)





1.5 Technical Specification

Table 1-2: AM4100 Main Specifications

AM4100		SPECIFICATIONS
Processor and Memory	CPU	The AM4100 supports the following microprocessors: • Freescale MPC8641D processor, 1.0 GHz, 400 MHz platform frequency • Freescale MPC8641D processor, 1.32 GHz, 528 MHz platform frequency • Freescale MPC8641D processor, 1.5 GHz, 600 MHz platform frequency All microprocessors are provided in a 1023 FC-CBGA packaging. Please contact Kontron for further information concerning the suitability of other Freescale processors for use with the AM4100.
	Memory	Main Memory: • Up to 2 GB unbuffered DDR2 SDRAM memory with ECC running at 600 MHz Cache structure: • 64 kB L1 on-die full speed processor cache • 32 kB for instruction cache for each core • 32 kB for data cache for each core • 1 MB L2 cache for each core NetBootLoader (NBL) Flash Memory: • Two redundant Firmware NOR Flash chips (2 x 4 MB) Mass Storage Device: • Up to 4 GB NAND Flash via an onboard IDE Flash Controller Serial EEPROM with 64 kbit
AMC Interconnection	Gigabit Ethernet	Common Options Region ports 0-1 • Two Gigabit Ethernet SerDes ports Front Panel • Two Gigabit Ethernet copper ports, or alternatively Fat Pipes Region ports 8-9 • Two Gigabit Ethernet SerDes ports (optional)
	PCI Express or Serial RapidIO	Fat Pipes Region ports 4-7 • One x4 PCI Express interface operating in root complex, or alternatively • One x4 Serial RapidIO interface operating in host or agent configuration
	Debug Interface	Extended Options Region port 14 • Reserved for debug port
	Serial Interface	Extended Options Region port 15 • One serial port
	Clock Input	Clocks • PCI Express clock reference input (FCLKA)
Connectors	Front Panel Connectors	• One serial port (SER0) with RS232-signal level on RJ45 connector • Two Gigabit Ethernet ports on RJ45 connectors
	AMC Card-edge Connector	• One 170-pin AMC Card-edge connector
Switches	DIP Switches	• One DIP switch consisting of four switches for board configuration, SW2 • One DIP switch consisting of two switches for IPMI FRU data selection, SW3

Table 1-2: AM4100 Main Specifications (Continued)

AM4100		SPECIFICATIONS	
LEDs	Module Management LEDs	- LED1 (red): Out-of-Service LED - LED2 (red/green/amber): Health LED - HS LED (blue): The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are <i>off</i>, <i>short blink</i>, <i>long blink</i>, and <i>on</i>.	
	User-Specific LEDs	- ULED3 (red/green): AMC Ethernet port A link signal status or POST code LED. - ULED2 (red/green): AMC Ethernet port B link signal status or POST code LED. - ULED1 (red/green): Freely configurable or POST code LED - ULED0 (red/green): Freely configurable or POST code LED	
Timer	Watchdog Timer	- Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 256 s in 12 steps - Serves for generating IRQ, hardware reset or both in cascaded mode	
	System Timer	- Two groups of four global 32-bit timers clocked with MPX clock or RTC clock input - Timers within each group can be joined to time longer durations - Hardware delay timer for short reliable delay times	
IPMI	Module Management Controller	- Renesas H8 microcontroller with 40 kB RAM and redundant 512 kB MMC Firmware Flash with automatic roll-back strategy - The MMC carries out IPMI commands such as monitoring several on-board temperature conditions, board voltages and the power supply status, and managing hot swap operations. - The MMC is accessible via a local IPMB (IPMB-L) and Keyboard Controller Style (KCS) Interfaces.	
	Hot Swap	The AM4100 has full hot swap capability.	
	Thermal Management	CPU and board overtemperature protection is provided by: - Four temperature sensors for monitoring the board temperature - CPU internal sensors - Specially designed heat sinks	
General	Power Consumption	For further information, refer to Chapter 6, "Power Considerations".	
	Temperature Range	Operational: -5°C to +55°C Storage: -40°C to +70°C	
	Mechanical	Single Module: - Mid-size version - Full-size version	
	Dimensions	Mid-size: 181.5 mm x 73.5 mm x 18.96 mm Full-size: 181.5 mm x 73.5 mm x 28.95 mm	
	Board Weight	Mid-size: 261 grams (with heat sink) Full-size: 304 grams (with heat sink)	
	JTAG	Two JTAG interfaces: - One processor JTAG interface routed to the onboard debug connector for debugging purposes - One onboard JTAG interface connected to the AMC Card-edge connector for debugging and manufacturing purposes	



Table 1-2: AM4100 Main Specifications (Continued)

AM4100		SPECIFICATIONS
Software	Firmware	Kontron NetBootLoader having the following features: • Terminal communication via the serial port on the front panel or via the AMC Card-edge connector • LAN boot capability for diskless systems (DHCP/BOOTP) • Plug and Play capability (PCI Express device enumeration) • NetBootLoader (NBL) Firmware parameters are saved in the EEPROM • Board serial number is saved within the EEPROM
	Software IPMI	Module Management Controller Firmware providing the following features: • The MMC is accessible via IPMB-L and KCS interfaces with interrupt support • The MMC Firmware can be updated in field through all supported interfaces using the free Linux Tool "IPMITool" • Two MMC Flash banks with automatic roll-back capability in case of an upgrade Firmware failure • Board supervision and control extensions such as board reset, power and NBL Firmware Flash control, and boot order configuration
	Operating Systems	The AM4100 is offered with various Board Support Packages. Please contact Kontron for further information concerning the operation of the AM4100 with other operating systems.

1.6 Kontron Software Support

Kontron is one of the few AdvancedTCA and CompactPCI vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.



1.7 Standards

The *Kontron* AMC boards comply with the requirements of the following standards.

Table 1-3: Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3 EN300386	--
	Immision	EN55024 EN61000-6-2 EN300386	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental and Health Aspects	Vibration (sinusoidal, operating)	GR-63-CORE EN300019-2-3 IEC61131-2 IEC60068-2-6	5-150 [Hz] frequency range 1 [g] acceleration 1 [oct/min] sweep rate 10 sweeps/axis 3 directions: x,y,z
	Vibration (random, transportation)	GR-63-CORE EN300019-2-2 IEC60068-2-64	5-20 [Hz]: 0.01[g ² /Hz] ASD 20-200 [Hz]: -3 [dB] slope 8.8 [m/s ² RMS] acceleration 30 [min] test time/axis 3 directions: x,y,z
	Shock (operating)	EN300019-2-3 IEC61131-2 IEC60068-2-27	15 [g] acceleration 11 [ms] pulse duration 3 shocks per direction 5 [s] recovery time 6 directions, ±x, ±y, ±z
	Permanent Shock (transportation)	EN300019-2-2 IEC60068-2-29	18 [g] acceleration 6 [ms] pulse duration 100 shocks per direction 1 [s] recovery time 6 directions, ±x, ±y, ±z
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment

**Note ...**

Kontron performs comprehensive environmental testing of its products in accordance with applicable standards.

Customers desiring to perform further environmental testing of Kontron products must contact Kontron for assistance prior to performing any such testing. This is necessary, as it is possible that environmental testing can be destructive when not performed in accordance with the applicable specifications.

In particular, for example, boards **without conformal coating** must not be exposed to a change of temperature exceeding 1K/minute, averaged over a period of not more than five minutes. Otherwise, condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

1.8 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
ATCA	PICMG® 3.0 AdvancedTCA Base Specification R2.0, March 18, 2005
MicroTCA	PICMG® MTCA.0 Micro Telecommunications Computing Architecture R1.0, July 6, 2006
AMC	PICMG® AMC.0, Advanced Mezzanine Card Specification R2.0 PICMG® AMC.1, PCI Express and Advanced Switching R1.0 PICMG® AMC.2, Gigabit Ethernet R1.0 PICMG® AMC.4, Serial RapidIO Draft 0.4
IPMI	IPMI - Intelligent Platform Management Interface Specification, v2.0 Document Revision 1.0, February 12, 2004 IPMI - Platform Management FRU Information Storage Definition, V1.0 Document Revision 1.1, September 27, 1999
PCI Express	PCI Express Base Specification Revision 1.0a
Serial RapidIO	RapidIO Interconnect Specification Revision 1.2



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Chapter

2

Functional Description



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2. Functional Description

2.1 Processor and Memory

2.1.1 Processor

The AM4100 supports the latest Freescale dual-core MPC8641D processor family up to speeds of 1.5 GHz with up to 600 MHz platform speed, such as:

- Freescale MPC8641D processor, 1.0 GHz, 400 MHz platform frequency
- Freescale MPC8641D processor, 1.32 GHz, 528 MHz platform frequency
- Freescale MPC8641D processor, 1.5 GHz, 600 MHz platform frequency

The MPC8641D processor includes two e600 cores each having 32 kB L1 instruction cache, 32 kB L1 data cache and 1 MB L2 cache. The processor further provides a DDR2 SDRAM memory controller, a local bus controller (LBC), a programmable interrupt controller (PIC), two I²C controllers, a four-channel DMA controller, and a dual universal asynchronous receiver/transmitter (DUART). For high-speed interconnect, the MPC8641D provides two sets of multiplexed pins that support two interface standards: 1x/4x Serial RapidIO (with message unit) and 1x/2x/4x/8x/ PCI Express. Furthermore, four integrated 10 Mbit/s, 100 Mbit/s and 1 Gbit/s Ethernet controllers offer TCP offload and classification capabilities. The MPC8641D processor delivers optimized power-efficient computing and outstanding dual-core performance with low power consumption and high system integration.

The MPC8641D processor supports symmetric multiprocessing (SMP) and asymmetric multiprocessing (AMP). SMP allows a platform to run one operating system on both cores. AMP allows a platform to run multiple operating systems and applications on the two cores independently from each other, for example, one real-time optimized operating system is run on the first core while the other core manages non-real-time tasks.

To enhance the CPU performance, each core of the MPC8641D is suited with a 64-bit floating-point unit (FPU) and the powerful AltiVec vector processing unit.

The following list sets out some of the key features of the Freescale MPC8641D dual-core processor:

- Two e600 cores with the following characteristics:
 - 32-bit, high-performance, superscalar microprocessor
 - 64-bit floating-point unit (FPU)
 - AltiVec support
 - L1 cache: two separate 32 kB instruction and data caches
 - L2 cache: integrated 1 MB, eight-way set-associative unified instruction and data cache with ECC support
- MPX coherency module (MCM)
- DDR2 memory controller:
 - 64-bit memory controller (72-bit with ECC)
 - Support for up to 600 MHz DDR2 SDRAM
- Serial RapidIO interface:
 - Compliant with the RapidIO Interconnect Specification Revision 1.2
 - 1x and 4x LP-serial link interfaces
 - Transmission rates of 1.25, 2.5 and 3.125 Gbaud (data rates of 1.0, 2.0 and 2.5 Gbps) per lane



- PCI Express interface:
 - Compliant with the PCI Express Base Specification Revision 1.0a
 - Support for x1, x2 and x4 link widths
 - 2.5 Gbaud, 2.0 Gbps lane
- Four identical enhanced three-speed Ethernet controllers (eTSECs):
 - Each TSEC incorporates a media access control sublayer (MAC) that supports 10 Mbps, 100 Mbps and 1 Gbps networks
 - Compliant with IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac and 802.3ab
 - Support of full-duplex FIFO mode for high-efficiency ASIC connectivity
 - TCP/IP Offload
 - Header parsing
 - Quality of service support
 - VLAN insertion and deletion
 - MAC address recognition
- Programmable interrupt controller (PIC) with support for PCI Express message shared interrupts (MSI)
- Local bus controller (LBC)
- Integrated four-channel DMA controller
- Device performance monitor
- Dual I²C controllers
- Dual universal asynchronous receiver/transmitter (DUART):
 - Two 4-wire interfaces (SIN, SOUT, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC 16550D
- IEEE 1149.1-compliant, JTAG boundary scan

2.1.2 Memory

The AM4100 supports a single-channel (72-bit), registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running up to 600 MHz (PC3200). The available memory configuration can be either 512 MB, 1 GB or 2 GB. ECC is able to correct single-bit errors and detect multiple-bit errors.

2.2 Peripherals

The following standard peripherals are available on the AM4100 board:

2.2.1 Timer

The AM4100 is equipped with the following timers:

- Real-Time Clock (RTC)

The AM4100 is equipped with an onboard high-precision real-time clock RV-8564-C2. The RV-8564-C2 RTC is register-compatible with the PCF8564A RTC from Philips/NXP. Additionally, it provides a very tight frequency tolerance at low power consumption. The AM4100 does not include a 3 V lithium battery or a GoldCap power source for RTC backup. The RTC can be powered from the management power. However, if this power is switched off, the RTC will lose its data.
- Hardware delay timer for short reliable delay times





2.2.2 Watchdog Timer

The AM4100 provides a Watchdog Timer that is programmable for a timeout period ranging from 125 ms to 256 s in 12 steps. Failure to trigger the Watchdog Timer in time results in an interrupt or a system reset. In the dual-stage mode, a combination of both interrupt and reset is generated if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog Timer generated the reset.

2.2.3 Power Monitor and Reset Generation

All onboard voltages on the AM4100 are supervised, which guarantees controlled power-up of the board. This is done by activating a stable power-up reset signals after the threshold voltages have been passed.

2.2.4 Flash Memory

There are three Flash devices available as described below, two for the NetBootLoader and one for the NAND Flash Disk Controller.

2.2.4.1 NetBootLoader Firmware Flash (NOR Flash)

The AM4100 provides two 4 MB, redundant NetBootLoader (NBL) Firmware Flash (MirrorBit® NOR Flash) chips. The fail-over mechanism for the Firmware recovery can be controlled via the MMC controller or the SW2 DIP switch.

If one NBL Firmware Flash is corrupted, the MMC can enable the second NBL Firmware Flash and boot the system again.

2.2.4.2 NAND Flash Disk Controller

The AM4100 supports up to 4 GB of NAND Flash memory in combination with the SST55LD019 NAND Flash Disk Controller, which is connected to the MPC8641D's local bus controller (LBC).

The SST55LD019 NAND Flash Disk Controller provides wear-leveling algorithm to extend the life expectancy of the connected NAND Flash.



2.3 Board Interfaces

2.3.1 Front Panel LEDs

The AM4100 is equipped with three Module Management LEDs and four User-Specific LEDs. The User-Specific LEDs can be configured via two onboard registers (see section 4.6.14, “User-Specific LED Configuration Register”).

Figure 2-1: Front Panel LEDs

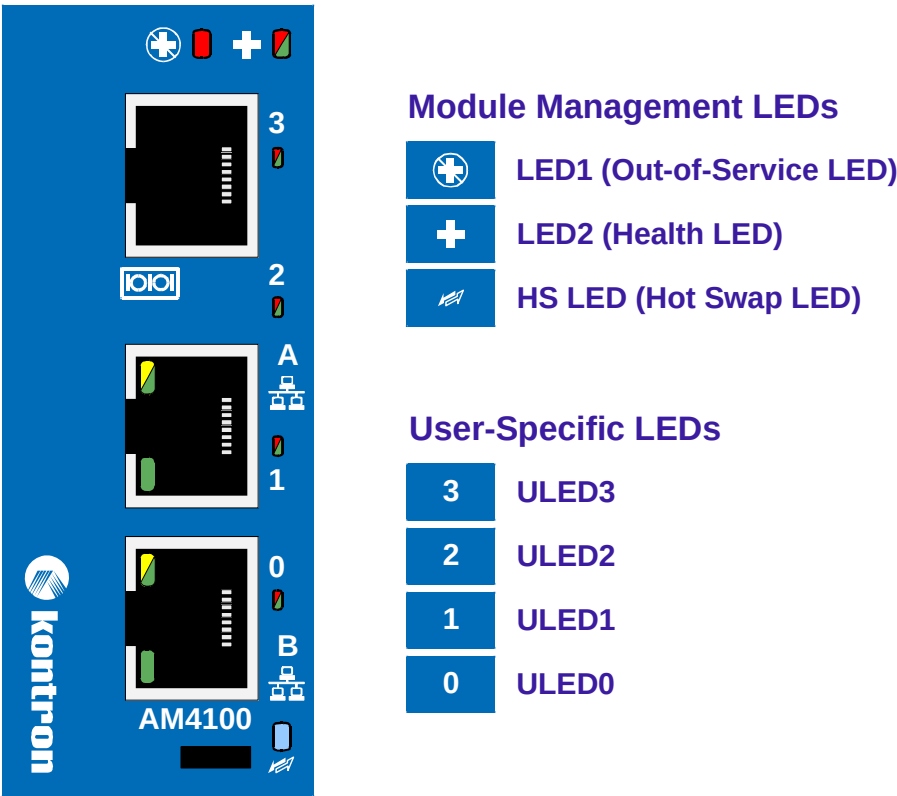




Table 2-1: Module Management LED Function

MODULE MANAGEMENT LED	COLOR	NORMAL MODE	OVERRIDE MODE state selectable by user or carrier, depending on PICMG LED command
LED1	red	Off = module powered / running	Depends on carrier or user
		On = module out of service	
		Pulsing = traffic on the IPMB-L bus	
LED2	red	Any action = health error detected	Depends on carrier or user
	green	Any action = no health error detected	
	red/green	Blinking slow = MMC running showing its heart beat Pulsing = KCS interface active	
HS LED	blue	On = ready for hot swap (module may be extracted) Blinking = how swap active (do not extract the module) Off = module in normal operation (do not extract the module)	By carrier: • On • Off • Slow/Fast Blinking By user: • Only lamp test

**Table 2-2: User-Specific LED Function**

USER-SPECIFIC LED	COLOR	FUNCTION DURING POWER-ON	FUNCTION DURING BOARD INITIALIZATION (IF POST CODE CONFIGURATION IS ENABLED)	DEFAULT FUNCTION AFTER POWER-ON
ULED3	red	When lit up during power-on, it indicates a power failure.	--	processor overtemperature above 105 °C
	green	--	POST bit 3 and bit 7	AMC Ethernet port A link signal status
ULED2	red	When lit up during power-on, it indicates a clock failure	--	processor overtemperature above 105 °C
	green	--	POST bit 2 and bit 6	AMC Ethernet port B link signal status
ULED1	red	When lit up during power-on, it indicates a hardware reset.	--	processor overtemperature above 105 °C
	green	--	POST bit 1 and bit 5	freely configurable (host or MMC)*
	red+green	--	--	freely configurable (host or MMC)*
ULED0	red	When lit up during power-on, it indicates a boot failure	--	processor overtemperature above 105 °C
	green	--	POST bit 0 and bit 4	freely configurable (host or MMC)*
	red+green	When lit up during power-on, it indicates a boot failure	--	freely configurable (host or MMC)*

* For further information regarding the configuration of the User-Specific LEDs, refer to section 4.6.14, "User-Specific LED Configuration Register".



How to Read the 8-Bit POST Code

The four User-Specific LEDs have been multiplexed in order to display 8-bit data. The following is an example of the User-Specific LEDs' operation if POST configuration is enabled (see also Table 2-2, "User-Specific LED Function").

Table 2-3: POST Code Example

STATE	USER-SPECIFIC LEDs
0	All User-Specific LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0



Note ...

Under normal operating conditions, the User-Specific LEDs should not remain lit during boot-up. They are intended to be used only for debug purposes. In the event that a User-Specific LED lights up during boot-up and the AM4100 does not boot, please contact the Kontron's Technical Support.

If all User-Specific LEDs flash red on and off at regular intervals, they indicate that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Once activated, the overtemperature event remains latched until a cold restart of the AM4100 is undertaken (all power off and then on again).



2.3.2 DIP Switches

The AM4100 is equipped with two DIP switches, one 4-bit general purpose DIP switch, SW2, and one 2-bit IPMI configuration DIP switch, SW3, both situated on the reverse side of the board. For further information, refer to chapter 4.1, Configuration of DIP Switches.

2.3.3 JTAG/Debug Interface

The AM4100 provides several onboard options for hardware and software debugging, such as:

- Four bicolor debug LEDs for signaling hardware failures and POST code
- An optional debug (processor JTAG) connector J5 (type: Hirose DF19G-20P-1H) is included to facilitate software debugging using an emulation probe

The following table provides pinout information for the debug connector J5.

Table 2-4: Debug Connector J5 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	3V3	Power supply	--
2	DEBUG_TDO	JTAG data output	O
3	DEBUG_TDI	JTAG data input	I
4	DEBUG_TRST	JTAG test reset	I
5	MODE	Factory use	I
6	DEBUG_TCK	JTAG test clock	I
7	DEBUG_CKSTP_IN	BDM/COP checkstop input	I
8	DEBUG_TMS	JTAG test mode select	I
9	DEBUG_SRST	BDM/COP soft reset	I
10	DEBUG_HRST	BDM/COP hard reset	I
11	DEBUG_CKSTP_OUT	BDM/COP checkstop output	O
12	GND	Ground signal	--
13	LPC_CLK	LPC clock	O
14	LPC_LFRAME	LPC frame	O
15	LPC_LAD0	LPC address/data	I/O
16	LPC_LAD1	LPC address/data	I/O
17	LPC_LAD2	LPC address/data	I/O
18	LPC_LAD3	LPC address/data	I/O
19	Res.	Reserved	--
20	Res.	Reserved	--



2.3.4 Serial Ports

The AM4100 provides two serial ports, SER0 and SER1, both fully compatible with the 16550 UART.

The SER0 interface provides receive and transmit signals as well as additional signals for handshaking mode. SER0 is available on the front panel as a serial RS232, 8-pin, RJ45, connector J4. Data transfer rates up to 115.2 kB/s are supported.

The SER1 interface provides only receive and transmit signals. SER1 is available on the AMC port 15 in the Extended Options Region of the AMC Card-edge connector as TTL 3.3 V signal level. Data transfer rates up to 115.2 kB/s are supported.

The following figure and table provide pinout information for the serial port connector J4.

Figure 2-2: Serial Con. J4 (SER0)

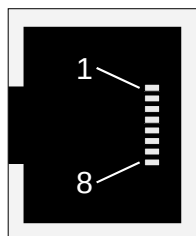


Table 2-5: Serial Con. J4 (SER0) Pinout

PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	Not used	Drives low	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	Not used	Reserved	I
8	CTS	Clear to send	I

2.3.5 Gigabit Ethernet Interfaces

The MPC8641D processor integrates four enhanced three-speed Ethernet controllers (eTSECs) complemented with an external BCM5466R QUAD Ethernet PHY. The PHY device supports 10BASE-T/100BASE-TX/1000BASE-T as well as 1000BASE-BX (SerDes) interfaces.

The Ethernet channels 1 and 3 of the MPC8641D are assigned to the AMC Base Interface as SerDes ports. Channels 2 and 4 can be directed to the front panel RJ45 connector. In certain board versions, these channels are configured as SerDes ports and directed to the AMC ports 8-9 in the Extended Options Region of the AMC Card-edge connector.

Two Gigabit Ethernet configurations are available on the AM4100:

- **Configuration with two Gigabit Ethernet TX interfaces on the front panel and two Gigabit Ethernet SerDes interfaces on the AMC Card-edge connector**

In this configuration two Gigabit Ethernet copper ports (1000BASE-TX) are connected to the RJ45 front panel connector and two Gigabit Ethernet SerDes ports are routed to the AMC ports 0-1 in the Common Options Region of the AMC Card-edge connector.

- **Configuration with four Gigabit Ethernet interfaces**

In this configuration two Gigabit Ethernet SerDes ports are routed to the AMC ports 0-1 in the Common Options Region of the AMC Card-edge connector and two additional Gigabit Ethernet SerDes ports are routed to the AMC ports 8-9 in the Fat Pipes Region of the AMC Card-edge connector.

2.3.5.1 Gigabit Ethernet Connectors

The Ethernet connectors, J2 and J3 are realized as RJ45 connectors. The interfaces provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

The J2 connector is connected to the MPC8641D's TSEC4 whereas J3 is connected to TSEC2.

Figure 2-3: Gigabit Ethernet Connectors J2/J3

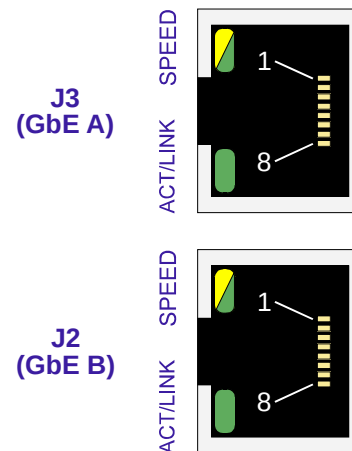


Table 2-6: Gigabit Ethernet Con. J2/J3 Pinout Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

SPEED (green/yellow): This LED lights up to indicate a successful 100Base-TX or 1000BASE-T connection. When green it indicates a 100Base-TX connection and when yellow it indicates a 1000Base-T connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.



2.4 AMC Interconnection

The AM4100 communicates with the carrier board or the MicroTCA backplane via the AMC Card-edge connector, which is a serial interface optimized for high-speed interconnects. The AMC Card-edge connector supports a variety of fabric topologies divided into five functional groups:

- Fabric interface
- Synchronization clock interface
- System management interface
- JTAG interface
- Module power interface

The following sections provide detailed information on these interfaces.

2.4.1 Fabric Interface

The Fabric interface is the real communication path and comprises 20 high-speed ports providing point-to-point connectivity for module-to-carrier and module-to-module implementations. The high-speed ports are separated in three logical regions as follows:

- Common Options Region
- Fat Pipes Region
- Extended Options Region

The AM4100 Port Mapping is described below and illustrated in figure 2-5.

- Common Options Region:
 - Ports 0-1: two Gigabit Ethernet SerDes ports
- Fat Pipes Region:
 - Ports 4-7: one x4 PCI Express interface operating as a root-complex, or alternatively one x4 Serial RapidIO interface operating in host or agent mode
 - Ports 8-9: two Gigabit Ethernet SerDes ports (optional)
- Extended Options Region:
 - Port 14: reserved for debug port
 - Port 15: one serial port



Figure 2-4: AM4100 Port Mapping

	Port No.	AMC Standard Port Mapping	AM4100 w/ x4 PCIe Port Mapping	AM4100 w/ x4 SIO Port Mapping
Basic Connector	TCLKA	Clocks	System Tick (optional)	System Tick (optional)
	TCLKB		not used	not used
	FCLKA		PCI Express Reference Clock	not used
	0	Common Options Region	GbE-A	GbE-A
	1		GbE-B	GbE-B
	2		not used	not used
	3		not used	not used
	4	Fat Pipes Region	x4 PCI Express	x4 Serial RapidIO
	5			
	6			
	7			
Extended Connector	8	Fat Pipes Region	GbE-C (optional)	GbE-C (optional)
	9		GbE-D (optional)	GbE-D (optional)
	10		not used	not used
	11	Extended Options Region	not used	not used
	12		not used	not used
	13		not used	not used
	14		Debug (LVTTL)	Debug (LVTTL)
	15		Serial (LVTTL)	Serial (LVTTL)
	TCLKC/D		not used	not used
	17			
	18			
	19			
	20			



2.4.2 Synchronization Clock Interface

On the AM4100, two PCI Express reference clock configurations are supported in accordance with the PCI Express Base Specification Revision 1.0a. One configuration uses two separate 100 MHz reference clocks, one on the AM4100 and one on the carrier. The other configuration uses one common clock source for both the AM4100 and the carrier. If the common clock source is used, the AM4100 uses the AMC clock interface FCLKA (see Figure 2-4, “AM4100 Port Mapping”). In this event, the carrier must provide the common reference clock (100 MHz) on the FCLKA pins.

2.4.3 System Management Interface

The system management interface is a port from the module to the carrier via the Local Intelligent Platform Management Bus (IPMB-L). The Module Management Controller uses this port for the communication with the Carrier Intelligent Platform Management Controller (IPMC). The IPMB-L is a multi-master I²C bus.

2.4.4 JTAG Interface

JTAG support is provided on the AMC Card-edge connector. The JTAG interface is supported for vendor product test and logic update. On the AM4100, the FPGA JTAG port is connected to the AMC JTAG port.

2.4.5 Module Power Interface

The module power interface provides the management power (MP) and payload power (PWR). These two supply voltages must have power-good indicators so that the system management can detect boot sequence events and nominal operating conditions.

The AM4100 operates with payload power in the range of 10.8 V to 13.2 V, and with management power of 3.3 V $\pm$ 5%.

The board supports removal and insertion in a powered slot as required by AMC.0.

2.4.6 Pinout of AMC Card-edge Connector J1

The AMC Card-edge connector is a high-speed serial interface and supports 170 pins. The following table provides pinout information for AMC Card-edge connector J1. The shaded table cells indicate signals that are not used on the AM4100.

Table 2-7: Pinout of AMC Edge Connector J1

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
1	GND	Logic Ground	-	170	GND	Logic Ground	-
2	PWR	Payload Power	Carrier	169	TDI	JTAG Test Data Input	Carrier
3	PS1#	Presence 1	AMC	168	TDO	JTAG Test Data Output	AMC
4	MP	Management Power	Carrier	167	TRST#	JTAG Test Reset Input	Carrier
5	GA0	Geographic Address 0	Carrier	166	TMS	JTAG Test Mode Select In	Carrier
6	RSV	Reserved (Optional PCIe Reset Output)	AMC	165	TCK	JTAG Test Clock Input	Carrier
7	GND	Logic Ground	-	164	GND	Logic Ground	-
8	RSV	Reserved	-	163	Tx20+	Not Connected	AMC
9	PWR	Payload Power	Carrier	162	Tx20-	Not Connected	AMC
10	GND	Logic Ground	-	161	GND	Logic Ground	-
11	Tx0+	GbE-A Transmitter +	AMC	160	Rx20+	Not Connected	Carrier
12	Tx0-	GbE-A Transmitter -	AMC	159	Rx20-	Not Connected	Carrier
13	GND	Logic Ground	-	158	GND	Logic Ground	-
14	Rx0+	GbE-A Receiver +	Carrier	157	Tx19+	Not Connected	AMC
15	Rx0-	GbE-A Receiver	Carrier	156	Tx19-	Not Connected	AMC
16	GND	Logic Ground	-	155	GND	Logic Ground	-
17	GA1	Geographic Address 1	Carrier	154	Rx19+	Not Connected	Carrier
18	PWR	Payload Power	Carrier	153	Rx19-	Not Connected	Carrier
19	GND	Logic Ground	-	152	GND	Logic Ground	-
20	Tx1+	GbE-B Transmitter +	AMC	151	Tx18+	Not Connected	AMC
21	Tx1-	GbE-B Transmitter -	AMC	150	Tx18-	Not Connected	AMC
22	GND	Logic Ground	-	149	GND	Logic Ground	-
23	Rx1+	GbE-B Receiver +	Carrier	148	Rx18+	Not Connected	Carrier
24	Rx1-	GbE-B Receiver -	Carrier	147	Rx18-	Not Connected	Carrier
25	GND	Logic Ground	-	146	GND	Logic Ground	-
26	GA2	Geographic Address 2	Carrier	145	Tx17+	Not Connected	AMC
27	PWR	Payload Power	Carrier	144	Tx17-	Not Connected	AMC
28	GND	Logic Ground	-	143	GND	Logic Ground	-



Table 2-7: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
29	Tx2+	Not Connected	AMC	142	Rx17+	Not Connected	Carrier
30	Tx2-	Not Connected	AMC	141	Rx17-	Not Connected	Carrier
31	GND	Logic Ground	-	140	GND	Logic Ground	-
32	Rx2+	Not Connected	Carrier	139	TCLKD+	Not Connected	AMC
33	Rx2-	Not Connected	Carrier	138	TCLKD-	Not Connected	AMC
34	GND	Logic Ground	-	137	GND	Logic Ground	-
35	Tx3+	Not Connected	AMC	136	TCLKC+	Not Connected	Carrier
36	Tx3-	Not Connected	AMC	135	TCLKC-	Not Connected	Carrier
37	GND	Logic Ground	-	134	GND	Logic Ground	-
38	Rx3+	Not Connected	Carrier	133	Tx15+	Serial Port Transmit	AMC
39	Rx3-	Not Connected	Carrier	132	Tx15-	Serial Port Receive	AMC
40	GND	Logic Ground	-	131	GND	Logic Ground	-
41	ENABLE#	AMC Enable	Carrier	130	Rx15+	Not Connected	Carrier
42	PWR	Payload Power	Carrier	129	Rx15-	Not Connected	AMC
43	GND	Logic Ground	-	128	GND	Logic Ground	-
44	Tx4+	PCIe-0 Transmitter + / Serial RapidIO-0 Trans- mitter +	AMC	127	Tx14+	Reserved for debug serial data output	AMC
45	Tx4-	PCIe-0 Transmitter - / Serial RapidIO-0 Trans- mitter -	AMC	126	Tx14-	Reserved for debug serial clock output	AMC
46	GND	Logic Ground	-	125	GND	Logic Ground	-
47	Rx4+	PCIe-0 Receiver + / Serial RapidIO 0 Receiver +	Carrier	124	Rx14+	Not Connected	Carrier
48	Rx4-	PCIe-0 Receiver - / Serial RapidIO 0 Receiver -	Carrier	123	Rx14-	Not Connected	Carrier
49	GND	Logic Ground	-	122	GND	Logic Ground	-
50	Tx5+	PCIe-1 Transmitter + / Serial RapidIO 1 Trans- mitter +	AMC	121	Tx13+	Not Connected	AMC
51	Tx5-	PCIe-1 Transmitter - / Serial RapidIO 1 Trans- mitter -	AMC	120	Tx13-	Not Connected	AMC
52	GND	Logic Ground	-	119	GND	Logic Ground	-

Table 2-7: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
53	Rx5+	PCIe-1 Receiver + / Serial RapidIO 1 Receiver +	Carrier	118	Rx13+	Not Connected	Carrier
54	Rx5-	PCIe-1 Receiver - / Serial RapidIO 1 Receiver -	Carrier	117	Rx13-	Not Connected	Carrier
55	GND	Logic Ground	-	116	GND	Logic Ground	-
56	SCL_L	IPMB-L Clock	IPMI Agent	115	Tx12+	Not Connected	AMC
57	PWR	Payload Power	Carrier	114	Tx12-	Not Connected	AMC
58	GND	Logic Ground	-	113	GND	Logic Ground	-
59	Tx6+	PCIe-2 Transmitter + / Serial RapidIO 2 Transmitter +	AMC	112	Rx12+	Not Connected	Carrier
60	Tx6-	PCIe-2 Transmitter - / Serial RapidIO 2 Transmitter -	AMC	111	Rx12-	Not Connected	Carrier
61	GND	Logic Ground	-	110	GND	Logic Ground	-
62	Rx6+	PCIe-2 Receiver + / Serial RapidIO 2 Receiver +	Carrier	109	Tx11+	Not Connected	AMC
63	Rx6-	PCIe-2 Receiver - / Serial RapidIO 2 Receiver -	Carrier	108	Tx11-	Not Connected	AMC
64	GND	Logic Ground	-	107	GND	Logic Ground	-
65	Tx7+	PCIe-3 Transmitter + / Serial RapidIO 3 Transmitter +	AMC	106	Rx11+	Not Connected	Carrier
66	Tx7-	PCIe-3 Transmitter - / Serial RapidIO 2 Transmitter -	AMC	105	Rx11-	Not Connected	Carrier
67	GND	Logic Ground	-	104	GND	Logic Ground	-
68	Rx7+	PCIe-3 Receiver + / Serial RapidIO 2 Receiver +	Carrier	103	Tx10+	Not Connected	AMC
69	Rx7-	PCIe-3 Receiver - / Serial RapidIO 2 Receiver -	Carrier	102	Tx10-	Not Connected	AMC
70	GND	Logic Ground	-	101	GND	Logic Ground	-



Table 2-7: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
71	SDA_L	IPMB-L Data	IPMI Agent	100	Rx10+	Not Connected	Carrier
72	PWR	Payload Power	Carrier	99	Rx10-	Not Connected	Carrier
73	GND	Logic Ground	-	98	GND	Logic Ground	-
74	TCLKA+	Telecom Clock A+ (optional)	Carrier	97	Tx9+	GbE-D Transmitter +	AMC
75	TCLKA-	Telecom Clock A- (optional)	Carrier	96	Tx9-	GbE-D Transmitter -	AMC
76	GND	Logic Ground	-	95	GND	Logic Ground	-
77	TCLKB+	Not Connected	AMC	94	Rx9+	GbE-D Receiver +	Carrier
78	TCLKB-	Not Connected	AMC	93	Rx9-	GbE-D Receiver -	Carrier
79	GND	Logic Ground	-	92	GND	Logic Ground	-
80	FCLKA+	PCIe Reference Clock +	Carrier	91	Tx8+	GbE-C Transmitter +	AMC
81	FCLKA-	PCIe Reference Clock -	Carrier	90	Tx8-	GbE-C Transmitter -	AMC
82	GND	Logic Ground	-	89	GND	Logic Ground	-
83	PS0#	Presence 0	Carrier	88	Rx8+	GbE-C Receiver +	Carrier
84	PWR	Payload Power	Carrier	87	Rx8-	GbE-C Receiver -	Carrier
85	GND	Logic Ground	-	86	GND	Logic Ground	-

**Warning!**

When handling the board, take care not to touch the gold conductive fingers of the AMC Card-edge connector.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.



The following table lists the reserved pins, which must not be connected to external circuitry.

Table 2-8: Reserved Pins Description

AMC PIN	AMC PORT	FUNCTION	I/O	SIGNALING VOLTAGE
6	--	Optional PCI Express reset output	O	3.3V TTL level
8	--	Reserved input for general purpose	I	3.3V TTL level



Warning!

The reserved pins listed above are reserved for optional use and must not be connected to external circuitry.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

The following table lists the Extended Options Regions pins:

Table 2-9: Extended Options Region Pins Description

AMC PIN	AMC PORT	FUNCTION	I/O	SIGNALING VOLTAGE
133	15	Tx serial port (SER1)	O	3.3V TTL level
132	15	Rx serial port (SER1)	I	3.3V TTL level
127	14	Reserved for debug serial data output	O	3.3V TTL level
126	14	Reserved for debug serial clock output	O	3.3V TTL level



Note ...

The Extended Options Region pins listed above are not differential signals. They have 3.3V TTL signaling voltage.

The following table lists the JTAG pins:

Table 2-10: JTAG Pins Description

AMC PIN	SIGNAL	FUNCTION	I/O	SIGNALING VOLTAGE
169	TDI	JTAG Test Data Input	I	3.3V TTL level
168	TDO	JTAG Test Data Output	O	3.3V TTL level
167	TRST#	JTAG Test Reset Input	I	3.3V TTL level
166	TMS	JTAG Test Mode Select In	I	3.3V TTL level
165	TCK	JTAG Test Clock Input	I	3.3V TTL level



Note ...

The JTAG pins are connected to the onboard FPGA logic and can be used to update the onboard logic. For further information, contact Kontron's Technical Support.



2.5 Module Management

A dedicated Module Management Controller (MMC) on the AM4100 manages the module and supports a defined subset of IPMI commands and sensors. For information on IPMI, refer to the IPMI FW User Guide for the AM4100 Module provided with the documentation CD.

2.5.1 Module Management Controller

The Module Management Controller is based on the 16-bit H8 microcontroller with three redundant 512 kB Flash blocks and 40 kB RAM. The redundant 512 kB Flash blocks provide an automatic roll-back strategy to the backup copy, for example, if a Firmware upgrade is interrupted or corrupted.

In addition to the code Flash, the field replacement unit (FRU) inventory information is stored in the nonvolatile memory on the EEPROM. It is possible to store up to 4 kB within the FRU inventory information.

The processor communicates with the MMC using the Keyboard Controller Style (KCS) interface. The address offset of the LPC KCS interface is 0xCA2, 0xCA3 and 0xCA0, 0xCA4. Furthermore, the MMC is able to communicate directly with the FPGA via the I²C interface. The I²C interface can be used to read the POST codes and configure the AM4100's default boot parameters.

The MMC is used to manage the AM4100, for example, it monitors several onboard temperature conditions, board voltages and the power supply status, manages hot swap LEDs and operations, reboots the board, etc. Additionally, the MMC can intervene in the operating status of the system by reading temperature values, shutting down systems, generating alarm signals if fault conditions occur. These fault conditions are simultaneously logged in the nonvolatile memory for analysis and for fault recovery.

To provide a reliable system, the AM4100 includes five temperature sensors distributed over the complete board to measure onboard temperature values and regulate the board's power consumption. The AM4100 uses the following temperature sensors:

- Inlet board temperature sensor near the AMC Card-edge connector (Inlet AMC Sensor)
- Outlet board temperature sensor near the AMC Card-edge connector (Outlet AMC Sensor)
- Inlet board temperature sensor near the processor (Inlet Processor Sensor)
- Outlet board temperature sensor near the processor (Outlet Processor Sensor)
- Freescale MPC8641D die temperature sensor (Processor Sensor)

The MMC also includes an integrated Watchdog to protect against CPU lockups. This enhances the board's characteristics and improves the system's reliability.

The MMC Firmware is designed and specially made for AMC environments, and is compliant with the PICMG 3.0 and IPMI v2.0 rev 1.0 specifications.

2.5.1.1 MMC Signals Implemented on the AM4100

The MMC implements several signals to monitor and control the different board functions. These signals are indicated in the following tables.

Table 2-11: Processor Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
PCI reset	Status of PCI reset signal	Monitor reset status
Board reset	Reset the complete board	Control reset circuit
Firmware Flash control	Firmware Flash fail-over control	Control Firmware Flashes
Post Code	POST code information	Monitor Startup Process
Boot order	Configure NetBootLoader boot order	Configure boot

Table 2-12: AMC-Specific Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
GA[0:2]	Geographic address	Monitor and control
Hot swap LED	Hot swap LED	Control LED
Hot swap switch	Status of hot swap switch	Monitor switch
User-specific LED	Basic feedback about failures	Control user-specific LED
Gigabit Ethernet A/B	Gigabit Ethernet link status	Monitor link status
Gigabit Ethernet C/D	Gigabit Ethernet link status	Monitor link status

Table 2-13: Onboard Power Supply Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
AMC power enable	Control AMC board supply	Control power supply
Onboard power supply	Status of various onboard supply voltages	Monitor power good signals
Processor power supply	Status of processor supply voltage	Monitor power good
Voltage 0.9 V	DDR2 termination supply	Monitor voltage
Platform Voltage	Board 1.1 V supply	Monitor voltage
Voltage 1.8 V	Board 1.8 V supply	Monitor voltage
Voltage 3.3 V	Board 3.3 V supply	Monitor voltage
Voltage 5 V	Board 5 V supply	Monitor voltage
Voltage AMC 3.3 V	AMC management power 3.3 V	Monitor voltage
Voltage AMC 12 V	AMC payload power 12 V	Monitor voltage



Table 2-14: Temperature Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
Processor temperature	Processor die temperature	Monitor temperature
Inlet AMC sensor temperature	Inlet board temperature sensor near the AMC Card-edge connector	Monitor temperature
Outlet AMC sensor temperature	Outlet board temperature sensor near the AMC Card-edge connector	Monitor temperature
Inlet processor temperature	Inlet board temperature sensor near the processor	Monitor temperature
Outlet processor temperature	Outlet board temperature sensor near the processor	Monitor temperature



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Chapter

3

Installation



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3. Installation

The AM4100 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AM4100. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until the board and heat sink have cooled down to room temperature.



Warning!

This AMC board is equipped with an extraction/locking handle which makes it possible to lock the board in a chassis/carrier during installation, or to unlock and pull it out of the chassis/carrier during removal. When installing or removing the board, apply only as much force as required to lock/unlock the board or to pull the board out of the chassis.

DO NOT push on the extractor/locking handle to seat the board in the AMC carrier/backplane connector.

Use of excessive force, bending or rotation of the handle will result in either damage to the handle or the board locking mechanism. Kontron disclaims all liability for damage to the board as a result of failure to comply with this warning.



ESD Equipment!

This AMC board contains electrostatic sensitive devices. Please observe the necessary precautions to avoid damage to the board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.



Warning!

This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

3.2 AM4100 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the AM4100 in a system.

To perform an initial installation of the AM4100 in a system, proceed as follows:

1. Ensure that the safety requirements indicated section 3.1 are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Before installation, ensure that the board is properly configured for operation in accordance with the application requirements. For information regarding the configuration of the AM4100, refer to Chapter 4.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AM4100 nor other system boards are physically damaged by the application of these procedures.

3. To install the AM4100, perform the following:
 1. Ensure that the board extractor/locking handle is fully extended away from the board.
 2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the AMC carrier/backplane connector. Using minimal force, apply pressure to the front panel until the board is seated in the AMC carrier/backplane connector.
 3. Using minimal force, push the extractor/locking handle towards the board until fully retracted.
 4. Connect all external interfacing cables to the board as required.
4. The AM4100 is now ready for operation. For operation of the AM4100, refer to the appropriate AM4100-specific software, application, and system documentation.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AM4100 nor other system boards are physically damaged when applying these procedures.

2. Ensure that no power is applied to the system before proceeding.



3. Disconnect any interfacing cables that may be connected to the board.

**Warning!**

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when removing the board.

4. Using minimal force, disengage the board from the AMC carrier/backplane connector by pulling on the extractor/locking handle until the board is disengaged.
5. After disengaging the board from the AMC carrier/backplane connector, pull the board out of the slot.
6. Dispose of the board as required.

3.4 AM4100 Hot Swap Procedures

The AM4100 is designed for hot swap operation. Hot swapping allows the coordinated extraction and insertion of modules without disrupting other operational elements within the system. This allows for identified faulty elements to be removed and replaced without taking the carrier card out of service that will typically be hosting other modules.

3.4.1 Hot Swap Extraction Procedures

To extract the board proceed as follows:

1. Ensure that the safety requirements indicated in section 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink.

**Warning!**

Care must be taken when applying the procedures below to ensure that neither the AM4100 nor other carrier boards are physically damaged by the application of these procedures.

2. The board's extractor/locking handle has three positions: retracted (locked), mid-position (hot swap microswitch disengaged), and extended (unlocked). During operation the handle is in the retracted position. In this position, the board is locked into the chassis/carrier and the hot swap microswitch is engaged.

To initiate hot swapping of the board, move the extractor/locking handle to the mid-position. Now, the following steps occur:

1. The BLUE HS LED begins to blink at short intervals
 - When the carrier IPMI controller receives the handle opened event, the carrier sends a command to the MMC with a request to perform short blinking of the BLUE HS LED. This indicates to the operator that the AM4100 is waiting to be deactivated.
 - Now the AM4100 waits for a permission from higher-level management (Shelf Manager or System Manager) to proceed with its deactivation.
 - Once the AM4100 receives the permission to continue the deactivation, all used ports are disabled.



- The Intelligent Platform Management Controller on the Carrier disables the AM4100's Payload Power.
2. The BLUE HS LED turns on steady
 - This indicates that the AM4100 may now be extracted.
 3. Disconnect any interfacing cables that may be connected to the AM4100.
 4. Move the extractor/locking handle to the extended (unlocked) position. Now, using minimal force, pull on the handle to extract the board.

**Warning!**

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Dispose of the board as required.

3.4.2 Hot Swap Insertion Procedures

The following procedures are applicable when inserting the AM4100 in a running system.

1. Ensure that the safety requirements indicated section 3.1 are observed.

**Warning!**

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installation. For information regarding the configuration of the AM4100 refer to Chapter 4.

**Warning!**

Care must be taken when applying the procedures below to ensure that neither the AM4100 nor other carrier boards are physically damaged by the application of these procedures.

3. To install the AM4100 perform the following:
 1. Ensure that the board extractor/locking handle is fully extended away from the board.
 2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the AMC carrier/backplane connector. Using minimal force, apply pressure to the front panel of the board until the board is seated in the AMC carrier/backplane connector.
 3. Connect all external interfacing cables to the board as required.
 4. Using minimal force, push the extractor/locking handle towards the board until fully retracted.



5. When the handle is fully retracted, the board is engaged and the following steps occur:

1. The BLUE HS LED turns on.

When the carrier recognizes that the AM4100 is fully seated, it enables the management power for the AM4100 and the BLUE HS LED turns on.

2. Long blinks of the BLUE HS LED

If the carrier IPMI controller detects the AM4100, it sends a command to the AM4100 to perform long blinks of the BLUE HS LED.

3. The BLUE HS LED turns off.

The Intelligent Platform Management Controller on the carrier reads the Module Current Requirements record and the AMC Point-to-Point Connectivity record. If the Module FRU information is valid and the carrier can provide the necessary payload power, the BLUE HS LED will be turned off. If the module FRU information is invalid or the carrier cannot provide the necessary payload power, the hot swap process is stopped and the BLUE HS LED keeps blinking. Should this problem occur, please contact Kontron's Technical Support.

4. Short blinks of the Module Management LEDs and the User-Specific LEDs

The carrier enables the payload power for the AM4100, and the Module Management LEDs and the User-Specific LEDs emit a short blink.

4. The AM4100 is now ready for operation. For operation of the AM4100, refer to appropriate AM4100-specific software, application, and system documentation.

3.5 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to the appropriate OS software documentation for installation.



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Chapter

4

Configuration



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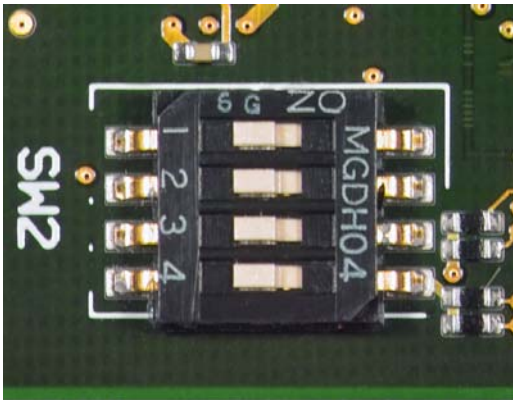
4. Configuration

4.1 Configuration of DIP Switches

4.1.1 SW2 DIP Switch Configuration

The General Purpose DIP switch, SW2, consists of four switches for board configuration: switch 1 for POST code or User-Specific LED configuration, switch 2 for NetBootLoader (NBL) Firmware Flash configuration, and switch 4 for configuring the low-memory address offset mode of the e600 core 1. Switch 3 is reserved for future use.

Figure 4-1: SW2 DIP Switch



The following table indicates the functions of the four switches integrated in the SW2 DIP switch.

Table 4-1: SW2 DIP Switch Functions

SWITCH	FUNCTION	DEFAULT
1	POST code or user-specific LED configuration	OFF
2	NetBootLoader Firmware Flash selection	OFF
3	Reserved	OFF
4	Core 1 LM Address Offset mode configuration	OFF



4.1.1.1 POST Code or User-Specific LED Configuration

The User-Specific LEDs are available for either general application use or for indicating the POST code value in the POST Code Register.

Table 4-2: POST Code or User-Specific LED Configuration

SWITCH 1	DESCRIPTION
OFF	<i>Enable POST Code configuration (User -Specific LED configuration disabled)</i>
ON	Enable User-Specific LED configuration (POST Code configuration disabled)

The default setting is indicated by using italic bold.

4.1.1.2 NetBootLoader Firmware Flash Configuration

For the NetBootLoader (NBL) Firmware there are two redundant NOR Flash chips on the AM4100 board. One chip is intended to provide a backup in the event that the other gets corrupted. If the currently used NetBootLoader Flash is corrupted due to physical damage or a faulty Flash upgrade, either the Module Management Controller or the SW2 DIP switch can select the redundant Flash, and the system can boot from it.

Switch 2 provides a hardware toggle function to force the onboard logic to switch from the currently used Flash to the redundant Flash. For example, if the switch is in the OFF position, switching to the ON position will force the use of the redundant Flash during the next boot operation.

Table 4-3: NetBootLoader Firmware Flash Configuration

SWITCH 2	DESCRIPTION
OFF	Toggle to the currently redundant NBL Firmware Flash when switching from ON to OFF.
ON	Toggle to the currently redundant NBL Firmware Flash when switching from OFF to ON.

4.1.1.3 Core 1 LM Address Offset Mode Configuration

Switch 4 controls the optional hardware Low-Memory Address Offset Mode for the e600 core 1. For further information on the Low Memory Address Offset Mode, refer to the respective section in the current Freescale's MPC8641D Integrated Host Processor Family Reference Manual.

Table 4-4: Core 1 Low Memory Address Offset Mode

SWITCH 4	DESCRIPTION
OFF	<i>Core 1 LM Address Offset Mode disabled (SMP)</i>
ON	Core 1 LM Address Offset Mode enabled (AMP)

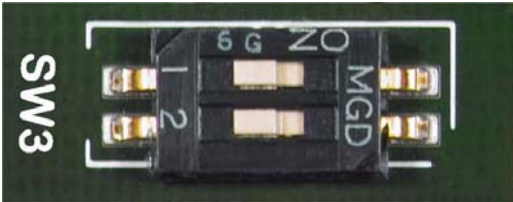
The default setting is indicated by using italic bold.



4.1.2 SW3 DIP Switch Configuration

The IPMI Configuration DIP switch, SW3, consists of two switches for selecting the FRU data set 0 sub-devices.

Figure 4-2: SW3 DIP Switch



The following table indicates the functions of the two switches integrated in the SW3 DIP switch.

Table 4-5: SW3 DIP Switch Functions

SWITCH 1	SWITCH 2	FUNCTION
OFF	OFF	Selects run mode: FRU data set 0, sub-device 0 (PCIe Root Complex)
ON	OFF	Reserved
OFF	ON	Selects run mode: FRU data set 0, sub-device 2 (sRIO Host)
ON	ON	Selects run mode: FRU data set 0, sub-device 3 (sRIO Agent)

For further information, refer to the IPMI FW User Guide for the AM4100 Module provided with the documentation CD.



4.2 JTAG Chain Configuration

The AM4100 provides three modes for JTAG chain configuration: JTAG test mode, emulator mode and emulator + logic only. For further information about configuring the JTAG chain using a hardware debugger, contact Kontron's Technical Support.

4.3 Interrupts

The AM4100 board uses the following IRQ routing.

Table 4-6: Interrupt Setting

IRQ	STANDARD FUNCTION
IRQ0	Reserved (PCIe1 INTA)
IRQ1	Reserved (PCIe1 INTB)
IRQ2	Reserved (PCIe1 INTC)
IRQ3	Reserved (PCIe1 INTD)
IRQ4	Reserved (PCIe2 INTA)
IRQ5	Reserved (PCIe2 INTB)
IRQ6	Reserved (PCIe2 INTC)
IRQ7	Reserved (PCIe2 INTD)
IRQ8	Watchdog Timer
IRQ9	KCS Serial Interrupt
IRQ10	NAND Flash Disk Controller
IRQ11	Reserved

4.4 Local Chip Select Line Usage

The MPC8641D processor provides eight local chip select (LCS) lines representing eight memory mapped areas. On the AM4100 the local chip select lines will be used according to the following table:

Table 4-7: Chip Select Line Usage

LCS	BUS WIDTH	CONTROLLED BY	DEVICE
LCS0	8	GPMC (general purpose chip select machine)	Board Registers + Startup code
LCS1	16	GPMC (general purpose chip select machine)	NOR-Flash 0 (at power-on)
LCS2	16	GPMC (general purpose chip select machine)	NOR-Flash 1 (at power-on)
LCS3	8	GPMC (general purpose chip select machine)	LPC Memory IP
LCS4	16	GPMC (general purpose chip select machine)	CompactFlash
LCS5	8	GPMC (general purpose chip select machine)	Core 1 startup code
LCS6	-	Not used	-
LCS7	-	Not used	-



4.5 Memory Map

The AM4100 board uses the following memory map.

Table 4-8: I/O Address Map

START ADDRESS	END ADDRESS	SIZE	LCS	WIDTH	DESCRIPTION
0x0_FFF0_8000	0x0_FFFF_FFFF	-	-	-	Not used
0x0_FFF0_0000	0x0_FFF0_7FFF	32kB	LCS5	8bit	Core 1 Startup Word
0x0_FE00_0000	0x0_FFEF_FFFF	-	-	-	Not used
0x0_FC00_0000	0x0_FDFF_FFFF (currently used Flash)	32MB	LCS1	16bit	NOR Flash 0 (NOR Flash 1)
0x0_F800_0000	0x0_FBFF_FFFF (redundant Flash)	64MB	LCS2	16bit	NOR Flash 1 (NOR Flash 0)
0x0_F400_0000	0x0_F7FF_FFFF	64MB	LCS3	8bit	LPC Memory
0x0_F000_0000	0x0_F3FF_FFFF	64MB	-	-	CCSRBAR
0x0_EC00_0000	0x0_EFFF_FFFF	64MB	LCS0	8bit	Board Registers + Startup Code
0x0_E800_0000	0x0_EBFF_FFFF	64MB	LCS4	16bit	CompactFlash
0x0_E000_0000	0x0_E7FF_FFFF	-	-	-	Reserved
0x0_C000_0000	0x0_DFFF_FFFF	512MB	-	-	Serial RapidIO
0x0_8000_0000	0x0_BFFF_FFFF	1GB	-	-	PCI Express
0x0_0000_0000	0x0_7FFF_FFFF	2GB	-	-	DDR2 SDRAM



4.5.1 Host CPU Register Map

The following table sets out the host CPU registers. The blue shaded table cells indicate MMC-specific registers.

Table 4-9: Host CPU Register Map

ADDRESS	DEVICE
0xEC00_0002	Memory Configuration Register
0xEC00_0008	Interface Configuration Register
0xEC00_0080	POST Code Registers
0xEC00_0280	Firmware Configuration Register
0xEC00_0281	MMC I/O Status Register
0xEC00_0282	Watchdog Timer Control Register
0xEC00_0283	AMC Geographic Addressing Register
0xEC00_0284	Board and Logic Revision Register
0xEC00_0285	Host Reset Status/Command Register
0xEC00_0286	Host I/O Status Register
0xEC00_0287	Host I/O Configuration Register
0xEC00_0288	Board ID Register
0xEC00_028A	Hot Swap Status Register
0xEC00_028B	User-Specific LED Configuration Register
0xEC00_028D	User-Specific LED Control Register
0xEC00_028E	Serial-over-LAN Configuration Register
0xEC00_028F	Delay Timer Control and Status Register
0xEC00_029C	MMC Configuration Register
0xEC00_0CA2 and 0xEC00_0CA3	IPMI SMS KCS interface
0xEC00_0CA0 and 0xEC00_0CA4	IPMI SMM KCS interface



4.6 Host CPU Registers

The following registers are special registers which the AM4100 uses to watch and/or configure the onboard hardware special features and the AMC control signals.

Normally, only the system Firmware uses these registers, but they are documented here for application use as required.



Note ...

Take care when modifying the contents of these registers as the NetBootLoader may be relying on the state of the bits under its control.

4.6.1 Memory Configuration Register

The Memory Configuration Register is used to inform the firmware about the memory of the AM4100.

Table 4-10: Memory Configuration Register

REGISTER NAME		MEMORY CONFIGURATION REGISTER		
ADDRESS		0xEC00_0002		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res	Reserved	0	R
6 - 5	MEM_SP	DDR2 memory speed: 00 = DDR2 400 MHz 01 = DDR2 528 MHz 10 = DDR2 600 MHz 11 = Reserved	N/A	R
4	ECC	Error Checking and Correcting: 0 = ECC not enabled 1 = ECC enabled	1	R
3	Res.	Reserved	0	R
2 - 1	MEM_SZ	Memory chip size: 00 = Chip size 256 Mbit 01 = Chip size 512 Mbit 10 = Chip size 1 Gbit 11 = Chip size 2 Gbit	N/A	R
0	MEM_BK	Memory bank: 0 = One physical bank is populated 1 = Two physical banks are populated	N/A	R



4.6.2 Interface Configuration Register

The Interface Configuration Register holds a series of bits defining the Ethernet, PCI Express (PCIe) and Serial RapidIO (sRIO) configurations.

Table 4-11: Interface Configuration Register

REGISTER NAME		INTERFACE CONFIGURATION REGISTER		
ADDRESS		0xEC00_0008		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	CFV	Configuration Valid: 0 = Configuration of registers not finished by MMC 1 = Configuration of registers finished by MMC	0	R
6 - 4	Res.	Reserved	000	R
3 - 1	SDT	CPU SerDes type: 000 = SerDes 1/2 disabled 001 = x4 PCIe 010 = Reserved 011 = Reserved 100 = Reserved 101 = sRIO 3.125 Gbit 110 = sRIO 1.25 Gbit 111 = sRIO 2.5 Gbit	N/A	R
0	SC	CPU SerDes configuration: 0 = PCIe end point / sRIO slave 1 = PCIe route complex / sRIO master	N/A	R



4.6.3 POST Code Register

The values stored in this register are displayed by the User-Specific LEDs when the switch 1 of SW2 DIP switch is set to OFF.

Table 4-12: POST Code Register

REGISTER NAME		POST CODE REGISTER		
ADDRESS		0xEC00_0080		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	PST	POST code output value	0x00	R/W

4.6.4 Firmware Configuration Register

The Firmware Configuration Register is used to configure a number of NBL Firmware settings. The register is read only and can be configured only by the Module Management Controller.

Table 4-13: Firmware Configuration Register

REGISTER NAME		FIRMWARE CONFIGURATION REGISTER		
ADDRESS		0xEC00_0280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-5	Res.	Reserved	000	R
4-3	BCON	Reserved	00	R
2-0	BBOCON	Reserved	000	R



Note ...

The Firmware Configuration Register is set to the default values by power-on reset, not by system reset.



4.6.5 MMC I/O Status Register

The MMC I/O Status Register describes the MMC control signals. The register is read only and can be configured only by the Module Management Controller.

Table 4-14: MMC I/O Status Register

REGISTER NAME		MMC I/O STATUS REGISTER		
ADDRESS		0xEC00_0281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	MFSEL	Reserved	1	R
6	MCHOT	MMC CPU overtemperature: 0 = CPU temperature is above 105°C 1 = Normal operation	1	R
5	MEOR	MMC AMC Extended Options Region configuration: 0 = AMC Extended Options Region is disabled 1 = AMC Extended Options Region is enabled With this bit the SER1 port and the debug port of the AMC Extended Options Region can be configured.	1	R
4	MFP89	MMC AMC Fat Pipes ports 8-9 configuration (GbE SerDes): 0 = AMC Fat Pipes ports 8-9 are disabled 1 = AMC Fat Pipes ports 8-9 are enabled With this bit the AMC Fat Pipes ports 8-9 can be configured.	0	R
3-1	Res.	Reserved	111	R
0	PEXC	PCI Express reference clock (100 MHz) configuration: 0 = Reference clock from AMC Card-edge connector (FCLKA) 1 = Local reference clock used	1	R



Note ...

The MMC Status I/O Register is set to the default values by power-on reset, not by system reset.



4.6.6 Watchdog Timer Control Register

The AM4100 has one Watchdog Timer provided with a programmable timeout ranging from 125 ms to 256 s. Failure to strobe the Watchdog Timer within a set time period results in a system reset or an interrupt.

There are four possible modes of operation involving the Watchdog Timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register (0xEC00_282) must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a '1' to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to '1'. What transpires after this depends on the mode selected.

The four operational Watchdog Timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a '1' to the WTR bit. In the event a timeout occurs, the WTE bit is set to '1'. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a '1' to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. To be effective, the hard reset must not be masked or otherwise negated. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.



Table 4-15: Watchdog Timer Control Register

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER		
ADDRESS		0xEC00_0282		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog timer expired status bit: 0 = Watchdog Timer has not expired 1 = Watchdog Timer has expired. Writing a '1' to this bit resets it to 0.	0	R
6-5	WMD	Watchdog Mode: 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable/Watchdog trigger control bit: 0 = Watchdog Timer has not been enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog Timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog Timer is enabled, it will indicate a '1'. 1 = Watchdog Timer is enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3-0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = reserved 1101 = reserved 1110 = reserved 1111 = reserved The nominal timeout period is 5% longer than the above-stated values.	0000	R/W



4.6.7 AMC Geographic Addressing Register

This register holds the AMC geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the AM4100.

Table 4-16: AMC Geographic Addressing Register

REGISTER NAME		AMC GEOGRAPHIC ADDRESSING REGISTER		
ADDRESS		0xEC00_0283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-5	Res.	Reserved	000	R
4-0	GA	AMC geographic address	N/A	R



Note ...

The AMC Geographic Addressing Register is set to the default values by power-on reset, not by PCI reset.

4.6.8 Board and Logic Revision Register

The Board and Logic Revision Register signals to the software when differences in the hardware require different handling by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each changed in hardware as development continues.

Table 4-17: Board and Logic Revision Register

REGISTER NAME		BOARD AND LOGIC REVISION REGISTER		
ADDRESS		0xEC00_0284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	HWR	Board revision	N/A	R
3-0	LR	Logic revision	N/A	R



4.6.9 Host Reset Status/Command Register

The Host Reset Status/Command Register is used to determine the system (host) reset source or force a system (host) reset.

Table 4-18: Host Reset Status/Command Register

REGISTER NAME		HOST RESET STATUS/COMMAND REGISTER		
ADDRESS		0xEC00_0285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PHRST	Power-on system (host) reset detection: 0 = System (host) reset generated by software (warm reset) 1 = System (host) reset generated by power-on (cold reset) Writing a '1' to this bit clears this bit.	N/A	R/W
6-5	Res.	Reserved	00	R
4	SYRST	Forced system (host) reset: 0 = No action 1 = Forced system (host) reset is generated	0	R/W
3	HMRST	System (host) reset generated by the MMC: 0 = System (host) reset generated by other reset source 1 = System (host) reset generated by MMC Writing a '1' to this bit clears the bit.	0	R/W
2-1	Res.	Reserved	00	R
0	HWRST	System (host) reset generated by the Watchdog timer: 0 = System (host) reset generated by other reset source 1 = System (host) reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W



4.6.10 Host I/O Status Register

The Host I/O Status Register describes the onboard and AMC control signals.

Table 4-19: Host I/O Status Register

REGISTER NAME		HOST I/O STATUS REGISTER		
ADDRESS		0xEC00_0286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-6	Res.	Reserved	00	R
5-4	FBSTA	Flash boot status: 00 = Boot from NOR Flash 0 NOR Flash 0 is mapped to LCS1 NOR Flash 1 is mapped to LCS2 01 = Boot from NOR Flash 1 NOR Flash 0 is mapped to LCS2 NOR Flash 1 is mapped to LCS1 10 = Reserved 11 = Reserved	00	R
3-0	DIPS	SW2 DIP Switch configuration	1111	R

4.6.11 Host I/O Configuration Register

The Host I/O Configuration Register holds a series of bits defining the onboard configuration.

Table 4-20: Host I/O Configuration Register

REGISTER NAME		HOST I/O CONFIGURATION REGISTER		
ADDRESS		0xEC00_0287		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-6	Res.	Reserved	00	R
5	FSEL	NOR Flash selection: Writing a 1 to this bit causes the currently used NOR Flash to become the redundant Flash, and, vice versa, the redundant Flash becomes the currently used NOR Flash	0	R/W
4-0	Res.	Reserved	00000	R

4.6.12 Board ID Register

This register describes the hardware and the board index. The content of this register is unique for each Kontron AMC board.

Table 4-21: Board ID Register

REGISTER NAME		BOARD I/D REGISTER		
ADDRESS		0xEC00_0288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-0	BID	Board identification: 0x47 = AM4100	0x47	R/W

4.6.13 Hot Swap Status Register

The hot swap status register describes the AMC hot swap handle status.

Table 4-22: Hot Swap Status Register

REGISTER NAME		HOT SWAP STATUS REGISTER		
ADDRESS		0xEC00_028A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res.	Reserved	0	R
6	HSH	Hot swap handle status: 0 = AMC hot swap handle in closed position 1 = AMC hot swap handle in open position	N/A	R
5-0	Res.	Reserved	000000	R

4.6.14 User-Specific LED Configuration Register

The User-Specific LED Configuration Register holds a series of bits defining the onboard configuration for the front panel User-Specific LEDs.

Table 4-23: User-Specific LED Configuration Register

REGISTER NAME		USER-SPECIFIC LED CONFIGURATION REGISTER		
ADDRESS		0xEC00_028B		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	Res.	Reserved	0000	R
3-0	ULCON	User-Specific LED Configuration: 0000 = POST ¹⁾ 0001 = MODE A ²⁾ 0010 = MODE B ³⁾ 0011 = MODE C ⁴⁾ 0100 - 1101 = Reserved 1110 = DIAG ⁵⁾ <i>This is the default mode after POST.</i> 1111 = TEST ⁶⁾	0000	R/W

Regardless of the selected configuration, the User-Specific LEDs are used to signal a number of fatal onboard hardware errors, such as:

ULED0: Firmware boot fail (red)
 ULED1: Hardware reset (red)
 ULED2: Clock fail (red)
 ULED3: Power fail (red)



¹⁾ In POST mode, the User-Specific LEDs build a binary vector to display the POST code during the pre-boot phase. In doing so, the higher 4-bit nibble of the 8-bit POST code is displayed, followed by the lower nibble, followed by a pause. The POST code is displayed in general in green color.

ULED0: POST bit 0 and bit 4 (green)
ULED1: POST bit 1 and bit 5 (green)
ULED2: POST bit 2 and bit 6 (green)
ULED3: POST bit 3 and bit 7 (green)

For further information on reading the 8-Bit POST Code, refer to section 2.3.1, "Front Panel LEDs".

²⁾ Configured for MODE A, the User-Specific LEDs are dedicated to functions as follows:

ULED0: User-Specific LED 0, controlled by HOST (red/green)
ULED1: User-Specific LED 1, controlled by HOST (red/green)
ULED2: Ethernet link status of AMC channel B (green)
ULED3: Ethernet link status of AMC channel A (green)

³⁾ Configured for MODE B, the User-Specific LEDs are dedicated to functions as follows:

ULED0: User-Specific LED 0, controlled by MMC (red/green)
ULED1: User-Specific LED 1, controlled by MMC (red/green)
ULED2: Ethernet link status of AMC channel B (green)
ULED3: Ethernet link status of AMC channel A (green)

⁴⁾ Configured for MODE C, the User-Specific LEDs are dedicated to functions as follows:

ULED0: Ethernet link status of AMC channel D (green)
ULED1: Ethernet link status of AMC channel C (green)
ULED2: Ethernet link status of AMC channel B (green)
ULED3: Ethernet link status of AMC channel A (green)

⁵⁾ Configured for DIAG, the User-Specific LEDs are dedicated to functions as follows:

ULED0: Watchdog Timer running (green), Watchdog Timer Timeout (red+green)
ULED1: TBD
ULED2: Ethernet link status of AMC channel B (green)
ULED3: Ethernet link status of AMC channel A (green)

⁶⁾ Configured for TEST, the User-Specific LEDs are dedicated to functions as follows:

ULED0: User-Specific LED 0 (red/green)
ULED1: User-Specific LED 1 (red/green)
ULED2: User-Specific LED 2 (red/green)
ULED3: User-Specific LED 3 (red/green)



4.6.15 User-Specific LED Control Register

The User-Specific LED Control Register enables the user to switch on and off the front panel User-Specific LEDs.

Table 4-24: User-Specific LED Control Register

REGISTER NAME		USER-SPECIFIC LED CONTROL REGISTER		
ADDRESS		0xEC00_028D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	ULCMD	User-Specific LED command: 0000 = Get User-Specific LED 0 0001 = Get User-Specific LED 1 0010 - 0111 = Reserved 1000 = Set User-Specific LED 0 1001 = Set User-Specific LED 1 1010 - 1111 = Reserved	0000	R/W
3-0	ULCOL	User-Specific LED color: 0000 = off 0001 = green 0010 = red 0011 = red+green 0100 = reserved 0101 = green, slow blinking 0110 = red, slow blinking 0111 = red+green, slow blinking 1000 = reserved 1001 = green, fast blinking 1010 = red, fast blinking 1011 = red+green, fast blinking	0000	R/W



Note ...

This register can only be used if the User-Specific LEDs indicated in the “User-Specific LED Configuration Register” (see Table 4-23) are configured in Mode A.



4.6.16 Serial-over-LAN Configuration Register

Via the Serial-over-LAN Configuration Register the MMC can configure a number of SOL settings. This register is read only and can be configured only by the MMC.

Table 4-25: Serial-over-LAN Configuration Register

REGISTER NAME		SERIAL-OVER-LAN CONFIGURATION REGISTER		
ADDRESS		0xEC00_028E		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	SCOM	Host SER0 port configuration for serial-over-LAN: 0000 = SER0 is routed to the front panel connector J4 0001 = SER0 is routed to the MMC serial port	0000	R
3-0	SOLC	Serial-over-LAN configuration: 0000 = the Serial-over-LAN function is not used 0001 = MMC is using host SER0 port for serial-over-LAN	0000	R



Note ...

If the MMC is using the host SER0 port for serial-over-LAN, both values, SCOM and SOLC, must be set to '0001'.

4.6.17 Delay Timer Control and Status Register

The delay timer enables the user to realize short, reliable delay times. It runs by default and does not start again on its own. It can be restarted at anytime by writing anything other than a '0' to the delay timer control/status register. The hardware delay timer provides a set of outputs for defined elapsed time periods. The timer outputs reflected in the Delay Timer Control and Status Register are set consecutively and remain set until the next restart is triggered again.

Table 4-26: Delay Timer Control and Status Register

REGISTER NAME		DELAY TIMER CONTROL/STATUS REGISTER																				
ADDRESS		0xEC00_028F																				
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS																		
7-0	DTC	Delay Timer Control The hardware delay timer is operated via one simple 8-bit control/status register. During normal operation, each of the 8 bits reflects a timer output which means defined elapsed time period after the last restart according to the following bit mapping: <table><tr><td>DTC[7:0]</td><td>Value</td></tr><tr><td>Bit 7:</td><td>1 ms</td></tr><tr><td>Bit 6:</td><td>500 μs</td></tr><tr><td>Bit 5:</td><td>250 μs</td></tr><tr><td>Bit 4:</td><td>100 μs</td></tr><tr><td>Bit 3:</td><td>50 μs</td></tr><tr><td>Bit 2:</td><td>10 μs</td></tr><tr><td>Bit 1:</td><td>5 μs</td></tr><tr><td>Bit 0:</td><td>1 μs</td></tr></table>	DTC[7:0]	Value	Bit 7:	1 ms	Bit 6:	500 μs	Bit 5:	250 μs	Bit 4:	100 μs	Bit 3:	50 μs	Bit 2:	10 μs	Bit 1:	5 μs	Bit 0:	1 μs	0x00	R/W
DTC[7:0]	Value																					
Bit 7:	1 ms																					
Bit 6:	500 μs																					
Bit 5:	250 μs																					
Bit 4:	100 μs																					
Bit 3:	50 μs																					
Bit 2:	10 μs																					
Bit 1:	5 μs																					
Bit 0:	1 μs																					

Since the timer width and thus the availability of outputs varies over different implementations, it is necessary to be able to determine the timer capability. Therefore, writing a '0' to the Delay Timer Control and Status Register followed by reading indicates the timer capability (not the timer outputs). For example, writing 0x00 and then reading 0xFF results in a 8-bit wide timer register. This status register mode can be switched to normal timer operation by writing anything other than a '0' to this register.



4.6.18 MMC Configuration Register

The MMC Configuration Register holds a series of bits defining the host serial port routing and the MMC serial port configuration.

Table 4-27: MMC Configuration Register

REGISTER NAME		MMC CONFIGURATION REGISTER		
ADDRESS		0xEC00_029C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	MPGC	MMC program request: 0 = No action 1 = Request MMC to program internal Flash from external Flash	0	R/W
6	MPGU	MMC enforce User Program Mode request: 0 = No action 1 = Set MMC in User Program Mode (this bit is ignored if MMC is in local programming mode)	0	R/W
5-4	Res.	Reserved	00	R
3	MCOMT	MMC serial port configuration for debugging purposes: 0 = MMC serial port is connected to the serial front panel RJ45 connector (only for debugging purposes) 1 = MMC serial port is isolated	1	R
2	MSCI	MMC serial port configuration for Firmware update: 0 = Host SER1 port is disable 1 = Host SER1 port is connected to MMC serial port (this bit is ignored if the MCOMT signal is 0)	0	R/W
1	MRST	MMC reset function: 0 = MMC controller is running 1 = MMC controller is in reset state	0	R/W
0	MPGM	MMC program mode; select the Firmware update mode: 0 = Normal operating mode 1 = Set MMC in firmware update mode	0	R/W

4.6.19 IPMI Keyboard Controller Style Interface

The host processor communicates with the MMC using two Keyboard Controller Style (KCS) interfaces, which are defined in the IPMI specification. One interface is for the System Management Software (SMS) used within an operating system, and one for the System Management Mode (SMM) used only by the NetBootLoader.

The KCS interface for the system management software is on the I/O location 0xEC00_0CA2 and 0xEC00_0CA3, and configured as regular ISA interrupt.

The KCS interface for the system management mode is on the I/O location 0xEC00_0CA0 and 0xEC00_0CA4, and configured as SMI interrupt.



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Chapter

5

NetBootLoader



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5. NetBootLoader

There are two NBL Flash memories (NBL-Flash0 and NBL-Flash1) available on the AM4100. These memories are identical and are redundant of one another. Only one of these Flash memories can be in use at any given time. The other is redundantly available, and, if required, it can be swapped with the currently used memory.

The AM4100 module is delivered with the NetBootLoader (NBL) software already programmed into both of the onboard soldered NBL Flash memory chips.

The NetBootLoader itself is a software utility which initializes the module for operation before turning control over to either an application or to an operator. This software also provides the capability to monitor and control the operation of the NetBootLoader itself, display system status information, to program executable code and data to the NBL Flash memory, and to load and start application software.

The following sections describe the functioning of the NetBootLoader and how to program the NBL Flash memory.

5.1 General Operation

Upon power on or a system reset, the NetBootLoader is started. The AM4100 is configured for operation and control is either passed to an application or an operator. In the event a valid image has been programmed into the NBL Flash memory and no operator or SCRIPT command intervention takes place, the image is copied into DDR2-SDRAM and control is passed to the application. If the NetBootLoader does not find a valid image or operator intervention has occurred, control is passed to the operator. The operator now has control to determine the system status, make configuration changes, read or program the NBL Flash memory, invoke the RUN command, or to restart or power the system down.

The operator command interfacing with the NetBootLoader is accomplished either via the SER0 serial port or one of the four Ethernet ports. During the boot operation a command interpreter is started which allows the operator to input commands to the NetBootLoader. Prior to interfacing via an Ethernet port, the port must be configured. This is done either via the SER0 serial port or via a DHCP/BOOTP server.

5.2 NetBootLoader Interfaces

There are three possibilities to interface with the NetBootLoader:

- Via the SER0 serial interface
- Via the SER1 serial interface
- Via an Ethernet port interface

Gaining access to the NetBootLoader is a function of the boot wait time setting, the contents of the script as defined by the SCRIPT command setting, and the availability of a valid image.

During the boot wait time, which is indicated by the user specific LED (ULED0) blinking green, the operator may intervene in the boot operation either by entering the ABORT command via the SER0 serial port, or by performing a successful telnet login via one of the Ethernet ports. If the operator does not intervene, the boot operation is continued after the boot wait time has been exceeded.



Once the boot wait time expires, an image must be copied to the DDR2-SDRAM, either via a script or from the contents of the NetBootLoader Flash, otherwise the boot operation is aborted. In the event the boot operation is aborted, control is passed to the command interpreter.

5.2.1 SER0 Serial Interface

The SER0 serial port is used to provide direct operator interfacing to the NetBootLoader. As soon as the AM4100 has been initialized this port is activated and the operator may input commands. During the boot wait time the operator may terminate the boot operation and take control of the NetBootLoader. Once the boot wait time is exceeded the command interpreter is normally deactivated and the boot process is continued. If the NetBootLoader does not copy an image to the DDR2-SDRAM, the boot process is discontinued and system control returns to the operator.

The SER0 serial interface may either be directly connected to a terminal device or may interface with a terminal emulator.

5.2.2 SER1 Serial Interface

The SER1 serial port is used to provide the NetBootLoader with the ability to access Motorola S-Records for programming an image to NBL Flash memory. No command interpreter is available for this interface.

5.2.3 Ethernet Port Interfaces

The Ethernet ports provide the capability of remote interfacing with the NetBootLoader. As the NetBootLoader only supports one of the four Ethernet ports, the port to be used must be configured prior to operation. Once configured it is available for remote operations as well as for accessing of TFTP/FTP file servers.

5.3 NetBootLoader Functions

In addition to initializing the AM4100 for operation and the loading and starting of applications, the NetBootLoader provides the following operator monitor and control functions:

- NetBootLoader control
- system status monitoring
- network accessing
- NBL Flash memory reading and programming operations
- Motorola S-Record acquisition

These functions are described in detail in the following chapters.



Note ...

The command title (CMD TITLE) is expressed in capital letters and is not the same as the syntax of the command. The command syntax is always written using small letters



5.3.1 NetBootLoader Control

The NetBootLoader provides various functions for controlling the operation of the NetBootLoader itself as well as the setting of operational parameters. The following table provides an overview of available NetBootLoader control functions.

Table 5-1: NetBootLoader Control Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
ABORT	-	Terminate boot wait	
BW	Boot Wait	Set or display boot wait time	
CBL	Change Bootline	Set or display a bootline	Applies to a specific kernel
DHCP	-	Dynamically set Ethernet port parameters	Requires that a DHCP or BOOTP server be available in the same network as the AM4100
FDT	-	Enable or disable FDT	Generates a flattened device tree for OS
HELP or ?	-	Display online HELP pages	
LOGOUT	-	Terminate telnet session	
NET	-	Manually set Ethernet port parameters	Must be set before attempting to use an Ethernet port; see also the DHCP command
PASSWD	Password	Set telnet password	Must be set before attempting telnet login
PF	Port Format	Set serial port parameters	Used for the SER0 and SER1 ports
RS	Reset	Resets system	
RUN	-	(Loads and) starts image	If image is not in the data buffer, it is first loaded then started
SCRIPT	-	Command scripting	Contents are executed only during boot up
SQ	Boot Sequence	Set or display boot sequence	Defines the image boot order



5.3.2 System Status Monitoring

The NetBootLoader provides various functions for monitoring the overall status of the system during the operation of the NetBootLoader. The following table provides an overview of available system status monitoring functions.

Table 5-2: System Status Monitoring Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CHECK	-	Image validation; displays information for each image	Verifies validity of user image programmed to NBL Flash memory
FDT_SHOW	-	Display FDT	
INFO	-	Display system information	
MD	Memory Display	Display memory contents	Applies to all memory
PCI	-	Display PCI device information	
PING	-	Verify network status	
VER	Version	Display version number of NetBootLoader	

5.3.3 Network Accessing

To support application development and operational requirements for various boot strategies, the NetBootLoader provides several functions for gaining access to network services. These functions include: access to DHCP/BOOTP servers, accessing TFTP servers, and accessing FTP servers.

At initial startup of the AM4100, only the NetBootLoader is installed in the NBL Flash memory. To support application development or remote boot capability, the NetBootLoader can provide network interfacing via an Ethernet port.

To achieve this, certain network parameters must first be configured. This can be done manually via a terminal or dynamically via the network. The command DHCP makes it possible to download such parameters and to configure an Ethernet port for network operation. Once the Ethernet port is configured, the commands TFTP and FTP are available to download bootable images or other files as required.

5.3.3.1 DHCP/BOOTP Server Access

Use of this access method requires the availability of either a DHCP or BOOTP server in the same network as the AM4100. The DHCP command causes the NetBootLoader to first attempt to establish contact with a DHCP server. If contact is not achieved, it then tries to contact a BOOTP server. When contact is established, parameters required by the AM4100 are provided accordingly and the Ethernet port is configured and then made available for normal operation.

In the event the AM4100 is reset or cold started the configuration parameters set by the above method are lost. Only if the parameters have been set by the NET command are they still available.

Prior to using the DHCP command, the IP address of the AM4100 must be set to 255.255.255.255 using the NET command.



5.3.3.2 TFTP/FTP Server Access

The NetBootLoader provides various functions for interfacing with either a TFTP or FTP server.

The TFTP server access is a simple method of acquiring a userimage from a remote source. Its primary use is to download a single executable image from a given source. For example, once an image has been created it would be possible to store it at a remote location where it then would be available for remote booting of an AM4100 via an Ethernet port.

The TFTP/FTP server commands provide various functions consistent with interfacing with such a server.

The following table provides an overview of available TFTP/FTP server functions.

Table 5-3: TFTP/FTP Server Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
BYE	-	Terminate session with FTP server	
CD	Change Directory	Change FTP server directory	
GET	-	Download a file from FTP server	Data buffer is target.
LOGIN	-	Login to FTP server	
LS	List Directory	List FTP server directory	Lists contents of directory.
PUT	-	Upload a file to FTP server	Data buffer is source.
PWD	Print Working Directory	Display current FTP server directory	Lists name of directory
TFTP	-	Download a file from TFTP server	Data buffer is target.

5.3.4 NBL Flash Operation

The NetBootLoader provides various functions for performing operations with the NBL Flash memory. The following table provides an overview of the available NBL Flash memory operation functions.

Table 5-4: NBL Flash Operation Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CLONE	-	Program NetBootLoader to NBL Flash memory	Uses data buffer as source
LF	Load Flash	Program image to NBL Flash memory	Uses data buffer as source
SF	Store Flash	Reads NBL Flash memory to data buffer	Uses data buffer as target
SWAP	-	Display or change current Flash assignment, and display Flash control parameters	Used to switch from the currently used NBL Flash to the currently redundant NBL Flash



5.3.5 Motorola S-Records

The NetBootLoader provides one function for acquiring Motorola S-Records. The following table provides an overview of this function.

Table 5-5: Motorola S-Records Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
SL	SLoad	Download Motorola S-Records	Uses data buffer as target

5.4 Operating the NetBootLoader

5.4.1 Initial Setup

The AM4100 is delivered with the NetBootLoader already installed in the NBL Flash memory and is ready for operation. However, in order for the AM4100 to be used in a system, application software must be made available for use. This may be accomplished by programming such an image also to the NBL Flash memory where the NetBootLoader is located.

Upon initial power up the NetBootLoader is started automatically. As soon as the NetBootLoader has completed initialization of the AM4100, it initiates a command interpreter which the operator can access either via the SER0 or an Ethernet interface. As long as the command interpreter is available, the operator has the opportunity to program an image.

Prior to programming an image it may be necessary to configure the NetBootLoader or perform other functions depending on the user's application development environment or application requirements. Once this has been accomplished and the image has been programmed, the AM4100 is ready for operation.

The following chapters provide information on how to set up and operate the NetBootLoader itself, initiation of the telnet interface, and how to program an image to the NBL Flash memory.

5.4.2 Accessing the NetBootLoader

Initial access to the NetBootLoader can only be achieved via the SER0 interface. Prior to using the telnet interface, the Ethernet port parameters must be set and this can only be accomplished initially via the SER0 interface.

The operator must either manually set the parameters using the net command or dynamically via the DHCP command. Prior to using the DHCP command, the IP address of the AM4100 must be set to 255.255.255.255 using the net command.

Once valid Ethernet port parameters and the telnet login password have been set, the telnet interface is available for operation.

Use of the SER0 interface requires either a terminal or a terminal emulator. Use of the telnet interface requires a remote telnet login to the NetBootLoader.

Availability of the command interpreter depends on the system status. If a valid image is not available, the command interpreter is active as long as the operator requires it. If a valid image is available, the command interpreter is only active for the duration of the boot wait time. If the operator requires the command interpreter for a longer time he must terminate the boot operation before the boot wait time is exceeded.



Upon initiation of the command interpreter, a prompt is sent to the SER0 interface and commands may be entered. To gain access to the NetBootLoader from a remote location via an Ethernet port, a telnet login must be performed. If the boot wait time has not been exceeded, a successful telnet login automatically terminates the boot operation and a command prompt is sent to the telnet remote interface.

Once the operator has control of the NetBootLoader, he may perform any required action. To continue with the operation of the AM4100, the system must either be cold started or the operator must issue a RESET command. In either event, the NetBootLoader is restarted and the boot operation begins anew.

5.4.3 NetBootLoader Configuration

There are several NetBootLoader commands which provide the operator with the capability to configure specific parameters which are used by the NetBootLoader for interfacing operations. These commands are:

- BW (BootWait)
- CBL (Change Bootline)
- DHCP
- FDT
- NET
- PASSWD
- PF (Port Format)
- SCRIPT
- SQ (Boot Sequence)

Default settings are available for all the above commands except for DHCP, NET, and SCRIPT.

5.4.3.1 BW

This command is used to display or set the actual boot wait time used by the NetBootLoader to delay the boot operation before proceeding with the loading and starting of an application. If this time is set too short it may not be possible to gain access to the NetBootLoader.

The boot wait time value is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.



Note ...

If the CRC of the boot section is not valid, changing the boot wait time will have no effect because the BW command does not validate an invalid CRC. In this case, a default timing of 5 seconds is always used.

To validate an invalid CRC, an operating system utility must be used, or, alternatively, the “-f” option of the BW command must be issued.



WARNING!

Using the “bw -f” command to validate invalid entries may adversely impact the operation of the operating system.



5.4.3.2 CBL

This command is used to set or display the bootline associated with a particular kernel image or which is common to all images.

5.4.3.3 DHCP

This command is used to obtain automatically networking parameters from either a DHCP or BOOTP server for an Ethernet port. Its use requires the availability of one or the other of these servers to function.

5.4.3.4 FDT

This command is used to disable or enable the creation of a flattened device tree.

The flattened device tree provides information required by certain operating systems for operation of system devices.

5.4.3.5 NET

This command is used to set or display the parameters for the configuration of the specified Ethernet port of the AM4100. The Ethernet interfaces are only available after these settings have been made.

5.4.3.6 PASSWD

This command is used to set the password used by the NetBootLoader for the operation of the telnet interface. No password is required for access from the SER0 interface.

5.4.3.7 PF

This command is used to set the port parameters for the SER0 and SER1 serial interfaces only for the current operator session. The next system restart will cause these settings to revert to the default settings of: 9600 Baud, 8 bits per character, 1 stop bit, and no parity. This is done to preclude a system lockout when restarting due to incompatible settings.

5.4.3.8 SCRIPT

This command permits the automatic invoking of NetBootLoader commands during boot up. The operator issues this command with appropriate options and then restarts the system. During the boot operation at boot wait time expiration, the script commands will be executed.

Use of this command permits, for example, remote booting from an TFTP server.



5.4.3.9 SQ

This command is used to set or display the order in which images are to be booted.

The NetBootLoader provides the capability to program up to four images into the NBL Flash memory. With this command the operator can define the order in which images may be used when the system is booted. This provides operational flexibility as well as the possibility for the system to compensate for a defective image.

For example, in the event the first image specified is defect, the NetBootLoader will attempt to load the next image specified. This is continued until either a valid image is loaded or no further image is available.

If no valid image is found, the NetBootLoader remains available for inputs.

5.4.4 telnet Login

A telnet login to the NetBootLoader is only possible during the boot wait time or when the boot operation has been terminated either by operator action or automatically by the NetBootLoader. In either case, the Ethernet port parameters and the telnet password must be set prior to attempting the telnet login.

To effect a telnet login the operator performs the standard telnet login procedure. The NetBootLoader responds by requesting a login password. The operator then enters a password. If the password is valid, the operator can now access the NetBootLoader. If the password is invalid, the telnet login procedure is terminated and the boot operation continues.

In the case of an invalid password, the login procedure may be repeated as often as required within the boot wait time or as long as the AM4100 telnet server is active after the boot wait time has been exceeded. Once the AM4100 telnet server is terminated, a telnet login is no longer possible.

5.4.5 NBL Flash Operations

To achieve an operable system for an application, the application software may be programmed to NBL Flash memory. As mentioned before, the NetBootLoader supports the programming of up to four images to NBL Flash memory whereby each image is assigned its own image number. In addition to this, it also supports the updating of the NetBootLoader itself as well as data transfer from the NBL Flash memory to the data buffer and from the data buffer to an FTP server. The following chapters provide information on performing the various types of NBL Flash memory operations.

5.4.5.1 NBL Flash Offsets

The currently used NBL Flash memory is one uniform Flash memory. All offsets are based from the beginning of this Flash memory area. The NetBootLoader itself is located at the beginning of the NBL Flash memory area and for this reason this area cannot be used for other image programming. To display an overview of the currently used NBL Flash memory organization use the INFO command.



If the image is an operating system (which is the default case), it must be programmed without an offset. When such an image is programmed to NBL Flash memory, the image length and CRC information is also programmed along with the image. This information is used by the NetBootLoader to determine the validity of the image during the boot operation. During system startup, a valid image is copied to DDR2-SDRAM address 0x0 and started at offset 0x0 (FDT enabled) or 0x100 (FDT disabled).

If an offset is specified, the image will be programmed exactly at this offset without adding length or CRC information. This option is intended for the storing of configuration information which is required to be located in NBL Flash memory.

When programming the NetBootLoader Flash memory using offsets (with the -o option), it is possible to unintentionally overwrite portions of previously programmed images. This may result in either an invalid image or erroneous data contents of the NetBootLoader Flash memory. It is recommended to first verify the contents of the NetBootLoader Flash memory using the INFO command before performing any programming with offsets. Refer to the INFO command for further information.

5.4.5.2 Programming an Image

The image itself must be compiled and linked to run from the DDR2-SDRAM base address 0x0 of the CPU. The entry point of the executable PPC code must be at offset 0x0 (FDT enabled) or 0x100 (FDT disabled).

Gaining access to the image for programming to NBL Flash memory depends on where it is located. The NetBootLoader can access four different sources for images:

- TFTP server
- FTP server
- Motorola S-Records
- memory within the visible address range of the AM4100

The NetBootLoader uses a single data buffer for downloading an image from a TFTP server, FTP server, or an image as Motorola S-Records. These images must first be downloaded to the data buffer prior to being programmed to NBL Flash memory. An image located within the visible address range of the AM4100 is directly accessible for programming.

To access an image located on a TFTP server, the TFTP command is used. To access an image located on an FTP server, the GET command is used. To perform Motorola S-Record acquisition, the SL (SLoad) command is used. Once the image is in the data buffer, the NBL Flash memory is programmed using the LF (Load Flash) command. For an image within visible memory, the LF command is used to program directly to NBL Flash memory.

5.4.5.3 Accessing TFTP and FTP Servers

To gain access to an image file stored on a TFTP or FTP server an Ethernet port is used. Images are downloaded to the data buffer using the FTP protocol. To use these interfaces, the Ethernet port parameters must first be set, and the operator must have control of the NetBootLoader.

To download an image from a TFTP server, the command TFTP is used. The TFTP server IP and file name of the image must be known and provided to the TFTP command or be provided by the DHCP server via the DHCP command.



To perform a download from an FTP server, the operator must first login to the FTP server. After a successful login, the operator then locates the image file required and downloads it to the data buffer. As with any type of server session, the operator should logout when the session is finished.

**Note ...**

The commands TFTP, GET, and LS use the same data buffer. Therefore if an LS command is issued after a TFTP or GET command the data buffer will be overwritten. If an LF command follows the LS the NetBootLoader refuses to program the overwritten data buffer to the NBL Flash memory.

5.4.5.4 Motorola S-Records

The NetBootLoader will also accept Motorola S-Records as an image. The SL command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

The checksum of every record except end records is checked. Bad records are rejected by the NetBootLoader. The address range of every record is also checked. Records which fall outside of the internal buffer are rejected.

The records must be 0-based. This means that each record's address must correspond to the address where it will be loaded in the data buffer relative to its start. If necessary, the base address can be modified with the -o option of the SL command.

**Note ...**

If the data buffer is programmed to NBL Flash memory without the -o option (program a startable image) the downloaded image is copied to RAM during startup and is executed there. For this reason images which require to be programmed must start at the address 0x0.

The image must start at the absolute address 0x0 and the entry point of the executable PPC code must be at address 0x0 (FDT enabled) or 0x100 (FDT disabled). If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses.

**Note ...**

Neither the SL nor LF command can be used to program Motorola S-Records to RAM areas.

For accessing the Motorola S-Records, both the SER0 and SER1 interfaces can be used. The user specific LED (ULED0) blinks green while downloading indicating that the transfer is in progress. The transfer itself may take several minutes to complete.

Ensure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, ensure that the host does not stop transmission after a number of lines (e.g. OS-9: use the 'nopause' attribute).

The SER0 and SER1 serial interface parameters can be modified with the PF command.



5.4.6 Updating the NetBootLoader

In addition to programming an image to NBL Flash memory, the NetBootLoader itself can be updated. The image is downloaded in the same way as any other image to the data buffer. The new version of the NetBootLoader image is then programmed to NBL Flash memory using the CLONE command.

5.4.7 Uploading an NBL Flash Memory Area

The NetBootLoader also has the possibility to upload certain areas of the NBL Flash memory to a host using an Ethernet port. To use this interface, the Ethernet port parameters must first be set and then the operator must gain control of the NetBootLoader and perform an FTP server login. After a successful login, the operator then stores the NBL Flash memory area to be uploaded to the local data buffer using the SF command. Using the PUT command transfers the contents of the data buffer to the FTP server. As with any type of server session, the operator should logout when the session is finished.

5.5 Plug and Play

The AM4100 NetBootLoader includes “Plug and Play” functionality. This ensures that the board is completely initialized and that all resources necessary for PCI devices (addresses, interrupts etc.) are assigned automatically. This important feature has the advantage that conflicts do not arise when PCI devices are added or removed as the operating system itself does not include the board initialization code.

5.6 Porting an Operating System to the CPU Board

The image for the absolute address 0x0 should be linked with an entry point at the absolute address 0x0 (FDT enabled) or 0x100 (FDT disabled).

One should not attempt to reassign the PCI BAR registers. The assigned values should be read back and these should always be used in the drivers.

Downloaded images are never executed from the NBL Flash memory. The programmed image is always downloaded to DDR2-SDRAM, the absolute address 0x0 being downloaded first. There is no configuration option available to amend this process. If it is necessary to relocate the image to another address after download, simply add a small assembly routine at the beginning of the code which will move the image to the correct address.



5.7 Commands

The following commands are available with the NetBootLoader. Where an ellipsis (...) appears in the command syntax it means that the command is continued from the previous line. Observe any spaces that may be between the ellipsis and the remainder of the command.

ABORT

FUNCTION:	Terminate the NetBootLoader boot operation
SYNTAX:	abort
DESCRIPTION:	This command is used by the operator to terminate the boot operation during the boot wait time to allow the operator to perform other NetBootLoader operations. To be asserted it must be issued during the boot wait time which is indicated by the user specific LED (ULED0) blinking green.

BW

FUNCTION:	Set or display the parameters of the boot wait function of the NetBootLoader
SYNTAX:	bw [<time> -f] where: bw command <time> parameter: numeric string 2, 5, 10, 20, 50 time in seconds, no other values than those above are supported -f option: force CRC update



BW

DESCRIPTION:	The command BW displays the parameter "<time>" setting. The parameter "<time>" stipulates the waiting time in seconds that the boot operation is delayed before the image is loaded and started. No values other than these are supported. Bear in mind when setting the boot wait time that the user specific LED (ULED0) blinks green slowly. Therefore, if the boot wait is set to 2 seconds the LED will only blink approximately four times. The option "-f" is used to force updating of the CRC value of boot section of the EEPROM. For further information refer to chapter 5.4.3.1.
USAGE:	Display setting of "<time>" parameter COMMAND / RESPONSE: bw WaitTime: 20
	Set boot wait time to 50 seconds COMMAND / RESPONSE (none): bw 50

BYE

FUNCTION:	Terminate an FTP server session
SYNTAX:	bye
DESCRIPTION:	An FTP server session which has been established with the command LOGIN is terminated with the command BYE.



CBL

	FUNCTION:	Set or display the parameters of the bootline function
	SYNTAX:	cbl [<num> (- <bootline>)] where: cbl command <num> parameter: string 0, 1, 2, 3, c ID number of the image to be associated with the bootline or bootline which is common to all images no other values than those above are supported - option: delete bootline for image specified or common <bootline> parameter: value: string (max. of 256 characters) <x ... x> defines the bootline to be used with the kernel indicated by <num> or the common bootline
	DESCRIPTION:	When an image is programmed to NBL Flash memory, it is assigned an ID number (0, 1, 2, or 3). This number is used to identify which image is to be addressed by the command CBL. In addition, a bootline common to all images may also be defined using the “c” parameter. If the command CBL is invoked without parameters, it returns the contents of all bootlines. Invoking the command CBL with the <bootline> parameter overwrites any previous bootline for the image specified.
	USAGE:	Display the bootline for image 2 COMMAND / RESPONSE: cbl <contents of all bootlines are displayed>

**CD**

FUNCTION:	Change the current FTP server directory
SYNTAX:	cd <new-path> where: cd command <new-path> parameter: string <x ... x> new directory path
DESCRIPTION:	If an FTP server session has been established with the LOGIN command, the command CD is used to change the current FTP server directory. The argument "<new-path>" may be an absolute or relative path. The format depends on what the server accepts. For example, UNIX hosts require that the directory names must be entered exactly in the same case.



CHECK

FUNCTION:	Verify validity of image programmed to NBL Flash memory
SYNTAX:	check
DESCRIPTION:	When an image is programmed to NBL Flash memory, a CRC is performed and the results are stored along with the image. The CHECK command provides status information for the current images in NBL Flash memory.
USAGE:	Verify valid image is stored in NBL Flash memory COMMAND / RESPONSE: check Checking Image: 0 check image crc: ok length in flash: 0x0053d004 sectors used : 84 Checking Image: 1 check image crc: ok length in flash: 0x0001029c sectors used : 2 Checking Image: 2 check image crc: fail length in flash: - sectors used : - Checking Image: 3 check image crc: fail length in flash: - sectors used : -



CLONE

FUNCTION:	Program the NetBootLoader to NBL Flash memory
SYNTAX:	clone -n [-a] [-y] where: clone command -n option: program from data buffer -a option: specifiy this option to program the currently used NBL Flash memory to program the redundant NBL Flash memory, do not specify this option -y option: this option is used with the SCRIPT command to confirm that cloning is to be performed
DESCRIPTION:	To update the NetBootLoader itself, the command CLONE is used. The image source for programming is the data buffer (-n). The image must first be downloaded to the data buffer. The new image is checked for validity. If an image is invalid, the update is aborted. Further, the operation must be confirmed by typing the word "yes". Any other or no input will cancel the operation. When used with the SCRIPT command, the -y option must be specified or the clone operation will be terminated.



CLONE

USAGE: Program NetBootLoader (normal operation)

COMMAND / RESPONSE:

```
NetBtLd> clone -n
clone: Fixup FLASH info from ftp buffer
This will overwrite the current ...
NetBootLoader in the fallback flash, are
you sure? [no] yes
clone: System transferred to fallback flash
NetBtLd>
```

Note: When responding to the overwrite query, "yes" must be spelled out. Any other response will terminate the cloning operation.

Program NetBootLoader (image not valid)

COMMAND / RESPONSE:

```
NetBtLd> clone -n
clone: Fixup FLASH info from ftp buffer
Image length invalid, image is damaged,
abort.
NetBtLd>
```



DHCP

FUNCTION:	Interface to a DHCP or BOOTP server; exchange network configuration parameters
SYNTAX:	dhcp [<timeout>] where: dhcp command <timeout> parameter: value: numerical string <[n ...]n> time, in seconds; must be ≥ 5 seconds
DESCRIPTION:	This command is used to set the network parameters for operation of an Ethernet port via either a DHCP or BOOTP server. Initially the AM4100 does not have a valid Ethernet interface configuration, and, therefore, this interface is inoperable. The initial configuration must be done either manually from the SER0 interface using the command NET, or, if a DHCP or BOOTP server is available, it can be done automatically by the DHCP command. Manually configured parameters are permanently stored. Parameters configured using the DHCP command are temporary and will be lost if the system is reset or cold started. Prior to using the DHCP command, the IP address must be set to 255.255.255.255 with the NET command.
USAGE:	Program NetBootLoader (normal operation) COMMAND / RESPONSE: NetBtLd> dhcp Sending request... reply from BOOTP/DHCP server. Network initialized ok. Server address is 192.168.112.2, our IP address is 192.168.112.14. Filename : NetBtLd>



FDT

FUNCTION:	Enable creation of a flattened device tree (FDT)
SYNTAX:	fdt [<switch>] where: fdt command <switch> parameter: numeric string 0,1 when set to 0 (zero) disables creation of an FDT, image is booted from 0x100 when set to 1 (one) enables creation of an FDT, image is booted from 0x0 when not specified, displays current setting
DESCRIPTION:	This command is used to specify the creation of an FDT for an operating system if required. An FDT is required for Linux kernels 2.6.17 and later.
USAGE:	Create an FDT COMMAND / RESPONSE: NetBtLd> fdt 1 Enabling creation of flattened device tree. Boot image from address 0. NetBtLd> Display the current FDT setting COMMAND / RESPONSE: NetBtLd> fdt Creation of flattened device tree is enabled. Image is booted from address 0. NetBtLd>



FDT_SHOW

FUNCTION:	Display the flattened device tree (FDT) information
SYNTAX:	fdt_show [<num>] where: fdt_show command <num> parameter: string 0, 1, 2, 3 ID number of the image for which FDT information is to be displayed no other values than those above are supported when not specified, displays FDT information for image 0
DESCRIPTION:	This command is used to have the NetBootLoader create and display the contents of the FDT for the image specified. The information provided can be used for system analysis or diagnostic purposes.



GET

FUNCTION:	Download file from FTP server
SYNTAX:	get <filename> where: get command <filename> parameter: string <x ... x> name of image file to be downloaded, or path and name of image file to be downloaded
DESCRIPTION:	To download a file from the FTP server to the local data buffer, the command GET is used. A successful FTP server login must be carried out before a file can be downloaded and the file must be in binary format. The argument "<filename>" must refer to an existing and accessible file on the server and the syntax must follow the requirements on the server, e.g. case sensitiveness. The argument may also include a path specification, if the server supports this.

HELP or ?

FUNCTION:	Display online help pages
SYNTAX:	help ?
DESCRIPTION:	This command displays the online help pages. The syntax of every command and a brief description is shown. The display output pauses after every page. The output can be continued with any key. Entering a "." (period) aborts the help function.



INFO

FUNCTION:	Display system information
SYNTAX:	info
DESCRIPTION:	The command INFO is used to display an information summary for the running system. Displayed are the following: CPU type, the board type, the size of the installed RAM and NBL Flash memory, and the areas occupied by the NetBootLoader and the programmed images. This information is displayed in hexadecimal offsets. Images programmed using the "-o" option of the command LF are not shown.
USAGE:	Display system information COMMAND / RESPONSE: <pre> info CPU : PowerPC, MPC8641D Board : AM4100 Ram : 20000000 Flash : Name : AMD 29LV320 Bank : 0 Bytelane : 0 BankPortsize : 16 ChipPortsize : 16 Offset : 0x0 Size : 0x400000 NetBootLoader used FLASH: 0x0 - 0x80000 Sector usage map: 0x0000: nnnnnnnn 00000000 0x0010: 00000000 00000000 0x0020: 00000000 00000000 0x0030: 00000000 0011.... Where: n = NetBootLoader; 0 = image 0; 1 = image 1; . = usage un- known </pre>



LF

FUNCTION:	Load Flash																		
SYNTAX:	<pre>lf [<num>] [[-r] [[-o[=<offset>] -k]]</pre> <pre>... [-m[=<adr>] -l[=<len>]]]</pre> where: <table><tr><td>lf</td><td>command</td></tr><tr><td><num></td><td>parameter: numeric string 0, 1, 2, 3 ID number assigned to this image</td></tr><tr><td>-r</td><td>option: delete image specified, or, if none specified, delete image 0</td></tr><tr><td>-o</td><td>option: offset <offset>parameter: hexadecimal <[x ...]x> program to FLASH offset of ...</td></tr><tr><td>-k</td><td>option: keep retain surrounding contents</td></tr><tr><td>-m</td><td>option: memory (address)</td></tr><tr><td><adr></td><td>parameter: hexadecimal <[x ...]x> absolute address of image to be programmed</td></tr><tr><td>-l</td><td>option: length</td></tr><tr><td><len></td><td>parameter: hexadecimal <[x ...]x> length of image to be programmed</td></tr></table>	lf	command	<num>	parameter: numeric string 0, 1, 2, 3 ID number assigned to this image	-r	option: delete image specified, or, if none specified, delete image 0	-o	option: offset <offset>parameter: hexadecimal <[x ...]x> program to FLASH offset of ...	-k	option: keep retain surrounding contents	-m	option: memory (address)	<adr>	parameter: hexadecimal <[x ...]x> absolute address of image to be programmed	-l	option: length	<len>	parameter: hexadecimal <[x ...]x> length of image to be programmed
lf	command																		
<num>	parameter: numeric string 0, 1, 2, 3 ID number assigned to this image																		
-r	option: delete image specified, or, if none specified, delete image 0																		
-o	option: offset <offset>parameter: hexadecimal <[x ...]x> program to FLASH offset of ...																		
-k	option: keep retain surrounding contents																		
-m	option: memory (address)																		
<adr>	parameter: hexadecimal <[x ...]x> absolute address of image to be programmed																		
-l	option: length																		
<len>	parameter: hexadecimal <[x ...]x> length of image to be programmed																		
DESCRIPTION:	If <num> is not specified, 0 is assumed. Without options, the NBL Flash memory is programmed using the contents of the data buffer. If no image is available in the data buffer, programming is terminated. If no offset option ("-o") is specified the image is added along with the CRC and length information. Normally, the local data buffer holds the image to be programmed. However, if the "-m" and "-l" options are specified, the image is programmed from the absolute address specified.																		



LF

DESCRIPTION:

If the “-o” option is specified, the contents are programmed exactly at this offset in NBL Flash memory. No length and no CRC information is added. In addition, no image number is assigned (even if specified), and the image cannot be loaded and started with the RUN command.

The “-k” option can be specified to prevent deletion of the surrounding NBL Flash memory contents.

Flash memory can only be erased sector-wise. If an image is programmed to a certain offset with the “-o” option, at least this sector (and maybe one or more of the following sectors depending on the size of the image) will be erased. The “-k” option can be used to retain the surrounding data, however, this slows down the operation significantly.

To achieve fast programming of parameter images without destroying other NBL Flash memory contents, the data should be placed at a sector boundary and the sector(s) must not contain any other data or executable images. If organized this way, use of the “-k” option can be avoided.

Note: The “lf” command cannot be used to program the NetBootLoader.

USAGE:

Program NBL Flash memory from data buffer and add CRC and image length (Image ID = 0 is assumed)

COMMAND / RESPONSE (none):

lf

Program NBL Flash memory from visible address at 0x87000000 for length of 0x123456

COMMAND / RESPONSE (none):

lf -m=87000000 -l=123456

Program NBL Flash memory from data buffer to offset 0xF4240 and retain adjacent NBL Flash memory contents

COMMAND / RESPONSE (none):

lf -o=f4240 -k

Delete image 1 from FLASH contents

COMMAND / RESPONSE (none):

lf 1 -r



LOGIN

FUNCTION:	Initiate FTP server session
SYNTAX:	login <ip-of-host> <username> [<password>] where: login command <ip-of-host> parameter: string <nnn.nnn.nnn.nnn> IP address of host <username> parameter: string <[x ...]x> FTP server user name <password> parameter: string <[x ...]x> user's password
DESCRIPTION:	The command LOGIN is used to establish an FTP server session. The "<password>" parameter is not necessary if the server does not require one.
USAGE:	Initiate FTP server session COMMAND / RESPONSE: login 192.168.47.12 johndoe mypassword (Response is dependent on the server accessed)

LOGOUT

FUNCTION:	Terminate telnet session with NetBootLoader
SYNTAX:	logout
DESCRIPTION:	A remote telnet session will be terminated with the command LOGOUT. No image is loaded and started if the session is terminated with LOGOUT. The NetBootLoader waits for a new session to be initiated or for a command entry from the serial console.



LS

FUNCTION:	Display listing of the current FTP server directory
SYNTAX:	ls
DESCRIPTION:	To display a listing of the current FTP server directory the command LS is used. This command downloads the listing to the data buffer and then the listing is displayed. Any previously loaded image in the data buffer is overwritten. If an attempt is then made to program the NBL Flash memory after the LS command has been issued it will fail.

MD

FUNCTION:	Display visible memory
SYNTAX:	md [<adr>] where: md command <adr> parameter: hexadecimal <[x ...]x> starting address of a visible memory area
DESCRIPTION:	To display a visible memory area the command MD is used. The first time the command MD is issued, visible memory contents starting at the address 0x0 are displayed if no "<adr>" parameter is used. If issued again without the "<adr>" parameter, the display starts with the end address of the previous display. Data is displayed as hexadecimal 32-bit words and as ASCII dump.



NET

FUNCTION:	Set or display the parameters for an Ethernet port																		
SYNTAX:	<pre>net [<num_net>] [<ip-addr>] ... [-netmask <netmask>] [-gw <gateway>] ... [-a] [-f]</pre> where: <table><tr><td>net</td><td>command</td></tr><tr><td><num_net></td><td>parameter: numerical string 0, 1 ... n logical identifier of Ethernet port addressed by this command where: 0 = TSEC1 1 = TSEC2 2 = TSEC3 3 = TSEC4</td></tr><tr><td><ip-addr></td><td>parameter: string <nnn.nnn.nnn.nnn> IP address of AM4100</td></tr><tr><td>-netmask</td><td>option: netmask</td></tr><tr><td><netmask></td><td>parameter: string <nnn.nnn.nnn.nnn> netmask of AM4100</td></tr><tr><td>-gw</td><td>option: gateway</td></tr><tr><td><gateway></td><td>parameter: string <nnn.nnn.nnn.nnn> gateway address for network</td></tr><tr><td>-a</td><td>option: specifies that the NetBootLoader is to use this port for network operations</td></tr><tr><td>-f</td><td>option: force CRC update</td></tr></table>	net	command	<num_net>	parameter: numerical string 0, 1 ... n logical identifier of Ethernet port addressed by this command where: 0 = TSEC1 1 = TSEC2 2 = TSEC3 3 = TSEC4	<ip-addr>	parameter: string <nnn.nnn.nnn.nnn> IP address of AM4100	-netmask	option: netmask	<netmask>	parameter: string <nnn.nnn.nnn.nnn> netmask of AM4100	-gw	option: gateway	<gateway>	parameter: string <nnn.nnn.nnn.nnn> gateway address for network	-a	option: specifies that the NetBootLoader is to use this port for network operations	-f	option: force CRC update
net	command																		
<num_net>	parameter: numerical string 0, 1 ... n logical identifier of Ethernet port addressed by this command where: 0 = TSEC1 1 = TSEC2 2 = TSEC3 3 = TSEC4																		
<ip-addr>	parameter: string <nnn.nnn.nnn.nnn> IP address of AM4100																		
-netmask	option: netmask																		
<netmask>	parameter: string <nnn.nnn.nnn.nnn> netmask of AM4100																		
-gw	option: gateway																		
<gateway>	parameter: string <nnn.nnn.nnn.nnn> gateway address for network																		
-a	option: specifies that the NetBootLoader is to use this port for network operations																		
-f	option: force CRC update																		



NET

DESCRIPTION:

To set or display the parameters of an Ethernet port the command NET is used.

Initially the AM4100 does not have any valid Ethernet port configurations, therefore, these interfaces are inoperable. The initial configuration of the Ethernet ports must be done from the SER0 interface using the command "net ... -f".

Using the "-f" option forces a CRC to be performed and stored along with the other configuration parameters in the serial EEPROM.

Once the configuration of an Ethernet port is done, it is available for operation. Later changes to the parameters do not require the use of the "-f" option to force a CRC. This is done automatically.

The <ip-addr> parameter must be set to 255.255.255.255 if the DHCP command is to be used for the configuration of the Ethernet interface.

If the NET command is issued without any parameters, the current parameter settings of all the Ethernet ports is displayed.



PASSWD

	FUNCTION:	Set the telnet password
	SYNTAX:	passwd [-f -d] where: passwd command -f option: if password is not known -d option: disable disable telnet login (remote access)
	DESCRIPTION:	To set the password for telnet sessions with the NetBootLoader the command PASSWD is used. This command is interactive, meaning that after it is issued, the NetBootLoader responds with an appropriate request to the operator which must be properly acknowledged or the operation fails (refer to USAGE below). To set the password in the event it is unknown, use the option “-f”. This is can only be accomplished from the SER0 interface and not from the Ethernet interface. With the option “-d”, the remote telnet login can be disabled by invalidating the password.
	USAGE:	Set password COMMAND / RESPONSE: NetBtLd> passwd Old Password: ***** New Password: ***** Type again : ***** NetBtLd> (The old password must be known)
		Set password when the old password is not known COMMAND / RESPONSE: NetBtLd> passwd -f New Password: ***** Type again : ***** NetBtLd>



PCI

FUNCTION:	Display PCI information
SYNTAX:	pci
DESCRIPTION:	The command PCI is used to display detailed information on all detected PCI devices. The bus number, device number, function number, vendor, and device ID's are displayed together with the configured base addresses and the assigned IRQ number.

PF

FUNCTION:	Set or display the serial port parameters (format)
SYNTAX:	pf [<port> [<baud>][/[<bitschar>] ...[/[<parity>][/<stops>]]]] where: pf command <port> parameter: string: "ser0" or "ser1" defines serial port to be configured <baud> parameter: numeric string: "300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400, 115200" defines the baud rate for the port <bitschar> parameter: numeric string: "7" or "8" defines the number of bits per character <parity> parameter: string: "n" (none), "o" (odd), "e" (even) defines parity to be used <stops> parameter: number string: "1" or "2" defines number of stop bits

**PF**

DESCRIPTION:	To set or display the operational parameters for the serial interfaces the command PF is used. At startup the settings for the SER0 and the SER1 interfaces are always set to the default values (9600/8/n/1). This is to avoid a possible system lockout. If other settings are required during operation of the NetBootLoader they may be made. If changes are made, it must be ensured that corresponding parameters are used for the operator console. Issuing this command without parameters being specified will display the current serial port settings. Syntax-wise, no spaces are permitted between the parameters and they must be separated with a slash. Not all parameters must be specified, but the "/" characters must be present to distinguish the different parameters from each other. The sequence can be aborted after every option.
	USAGE: Set SER0 to 300 Baud, 7 Bits/char, odd parity, and 2 stop bits COMMAND / RESPONSE (none): pf ser0 300/7/o/2
	Set the bits per character parameter of SER1 to 7 COMMAND / RESPONSE (none): pf ser1 //7
	Set the stop bits parameter of SER1 to 2 COMMAND / RESPONSE (none): pf ser1 ///2



PING

FUNCTION:	Verify operability of an Ethernet interface																
SYNTAX:	<pre>ping <ip_addr> [-c <count>] [-s <size>] ... [-w <wait>]</pre> where: <table> <tr> <td>ping</td><td>command</td></tr> <tr> <td><ip-addr></td><td>parameter: string <nnn.nnn.nnn.nnn> IP address of target</td></tr> <tr> <td>-c</td><td>option: count</td></tr> <tr> <td><count></td><td>parameter: numeric string <[n ...]n> number of packets to send</td></tr> <tr> <td>-s</td><td>option: size</td></tr> <tr> <td><size></td><td>parameter: numeric string <[n ...]n> size of packet to send in bytes</td></tr> <tr> <td>-w</td><td>option: wait</td></tr> <tr> <td><wait></td><td>parameter: numeric string <[n ...]n> wait time between packets in seconds</td></tr> </table>	ping	command	<ip-addr>	parameter: string <nnn.nnn.nnn.nnn> IP address of target	-c	option: count	<count>	parameter: numeric string <[n ...]n> number of packets to send	-s	option: size	<size>	parameter: numeric string <[n ...]n> size of packet to send in bytes	-w	option: wait	<wait>	parameter: numeric string <[n ...]n> wait time between packets in seconds
ping	command																
<ip-addr>	parameter: string <nnn.nnn.nnn.nnn> IP address of target																
-c	option: count																
<count>	parameter: numeric string <[n ...]n> number of packets to send																
-s	option: size																
<size>	parameter: numeric string <[n ...]n> size of packet to send in bytes																
-w	option: wait																
<wait>	parameter: numeric string <[n ...]n> wait time between packets in seconds																
DESCRIPTION:	To verify the operational status of an Ethernet interface the command PING is used. This command tests the network connection and target server's ability to respond. If no other parameters are specified, four requests will be sent. This can be changed with the parameter "-c". The typical size of a ping packet can be changed with the parameter "-s" and the time between requests, which is typically one second, can be changed with the parameter "-w". Responses to the PING command are dependent on the performance of the network.																
USAGE:	Send ten packets, 100 bytes long, and wait two seconds between packets COMMAND / RESPONSE: <pre>ping 192.192.158.7 -c 10 -s 100 -w 2</pre>																



PUT

FUNCTION:	Upload contents of the data buffer to the FTP server
SYNTAX:	put <filename> where: put command <filename> parameter: string <x ... x> file name to be used for contents of data buffer to be uploaded
DESCRIPTION:	To upload the contents of the data buffer to a file on an FTP server, the command PUT is used. The file indicated by the parameter "<filename>" is created on the server. In the event that a file with this name already exists, its contents will be overwritten.

PWD

FUNCTION:	Display the current FTP server directory path
SYNTAX:	pwd
DESCRIPTION:	If a FTP connection has been established with the LOGIN command, the command PWD is used to display the complete path of the current directory on the FTP server.



RS

FUNCTION:	Reset the system
SYNTAX:	rs
DESCRIPTION:	To permit the operator to force a restart of the system, the command RS is used. This command terminates the NetBootLoader command interpreter and resets the entire system. If this command is issued over a remote telnet connection, the telnet session is terminated prior to the generation of the reset.

RUN

FUNCTION:	(Loads and) starts a bootable image
SYNTAX:	run [<num>] where: run command <num> parameter: string 0, 1, 2, 3 ID number of the image to be booted no other values than those above are supported if no image is specified, the image in the data buffer is booted
DESCRIPTION:	This command is used to (load and) start a boot image.



SCRIPT

FUNCTION:	Provides very basic scripting capability
SYNTAX:	script [<newscript> -] where: script command <newscript> parameter: string <[x ...]x> “<newscript>” may only include NBL commands; flow control constructs are not permitted; com- mands must be separated by semi-colons - option: delete script contents
DESCRIPTION:	With the SCRIPT command, it is possible to control the boot process. During booting, if a valid script is available, the NetBootLoader will process it once the boot wait time is expired. If this command is issued without any parameters, the currently active script contents are displayed.
USAGE:	Download a boot image from a TFTP server and run the boot image. COMMAND / RESPONSE (none): script dhcp; tftp; run Upon the next reset or cold start, after the boot wait time has expired the commands DHCP, TFTP, and RUN will be executed in that order. The above command sequence configures an Ethernet port, downloads the specified bootable image from an TFTP server, and then starts this image.



SF

FUNCTION:	Store NBL Flash memory contents to data buffer
SYNTAX:	<pre>sf (-o[=<offset>] -l[=<length>]) ...(-m[=<add>] -l[=<length>]) ...(<num>[-o[=<offset>]][-l[=<length>]])</pre> where: - sf command -o option: offset <offset> parameter: value: hexadecimal relative offset to start of FLASH contents or image to be stored to the data buffer -l option: length <length> parameter: value: hexadecimal length of FLASH contents or area of visible mem- ory to be stored to the data buffer -m option: memory (address) <adr> parameter: hexadecimal <[x ...]x> absolute address of image to be programmed <num> parameter: numerical string 0, 1, 2, 3 number of the image to be stored
DESCRIPTION:	With the command SF a selected portion of the NBL Flash memory contents may be copied to the local data buffer, e.g. for a subsequent upload to the FTP server with the PUT command.
USAGE:	Store 64 kB of NBL Flash memory contents to the data buffer beginning at an offset of 1 MB COMMAND / RESPONSE (none): <pre>sf -o=100000 -l=10000</pre> Store FLASH image 2 to the data buffer COMMAND / RESPONSE (none): <pre>sf 2</pre>



SL

	FUNCTION:	Download Motorola S-Records to data buffer
	SYNTAX:	sl [-o[=<offset>]][-u] where: sl command -o option: offset <offset> parameter: hexadecimal: unsigned <[x ...]x> offset to be subtracted from each record's address -u option: source = SER1 instead of SER0
	DESCRIPTION:	With the command SL Motorola S-Records are downloaded to the data buffer and the record addresses modified accordingly as required for DDR2-SDRAM operation (for copying to 0x0). The "<offset>" parameter may be used to change the record base to 0x0. The "-u" option selects the SER1 interface as source for the S-Records, otherwise the SER0 interface is used.
	USAGE:	Download S-Records to data buffer and reduce each record's address by 0x10000. COMMAND / RESPONSE (none): sl -o=10000



SQ

FUNCTION:	Set or display the boot sequence
SYNTAX:	sq [<num1><num2><num3><num4>] where: sq command <num1> parameter: numeric string: "0, 1, 2, 3" ID number of image to be booted <num2> parameter: numeric string: "0, 1, 2, 3" ID number of image to be booted <num3> parameter: numeric string: "0, 1, 2, 3" ID number of image to be booted <num4> parameter: numeric string: "0, 1, 2, 3" ID number of image to be booted
DESCRIPTION:	Up to four bootable images may be programmed into the NBL Flash memory. The boot sequence defines to the NetBootLoader the order in which images are to be accessed when booting. The NetBootLoader starts with "<num1>" and continues until a valid image is found. In the case that a valid image is not found, the NetBootLoader stops searching and waits for operator intervention. All four number parameters must be defined even if there is not an image in the NBL Flash memory with that ID number. Any given ID number may only be used once: e.g. a sequence of 0120 is not permitted. The default sequence is 0123 if the boot sequence has not been programmed.
USAGE:	Display the current boot sequence setting. COMMAND / RESPONSE: sq <cr> Bootsequence: 0 - 3 - 1 - 2
	Set the boot sequence to 3201. COMMAND / RESPONSE(none): sq 3201



SWAP

	FUNCTION:	Modify or display the current NBL Flash memory device usage
	SYNTAX:	swap [-t -p] where: swap command -t option: temporary temporary NBL Flash swap -p option: permanent permanent NBL Flash swap
	DESCRIPTION:	The configuration of the NBL Flash memory devices (currently used or redundant) is controlled by the IPMI controller, the payload (HOST), and the switch SW2 (DIP switch position 2). The setting combination of all three determines the current configuration. The SWAP command is a toggle function meaning that when the configuration is to be swapped, the SWAP command is invoked with the “-t” option (temporary, at the next power on the configuration reverts to the previous setting) or the “-p” option (permanently). The current configuration can be determined by invoking the SWAP command without either option. If the board is not operated in a ATCA or μTCA environment (e.g. on the AMEVAL1), startup problems may arise due to the simultaneous startup of the payload (CPU) and the MMC. If the assignment is configured as 'IPMI: reverse', the MMC switches the flashes during payload startup which normally causes a crash. This can be circumvented by holding the payload startup with a debug probe for a few seconds or by delaying the startup of the MMC (switch 'AMC ENABLE' on the AMEVAL1) and then switching back to 'IPMI: straight' once the system is running.



SWAP

USAGE: Swap the NBL Flashes temporarily and verify

COMMAND / RESPONSE:

```
NetBtLd> swap -t
```

```
Flash config swapped till next reboot via  
HOST bit
```

```
NetBtLd>
```

```
NetBtLd> swap
```

```
Active   Flash is NOR flash 1
```

```
Fallback Flash is NOR flash 0
```

Configuration Details:

```
IPMI    : straight
```

```
HOST    : reverse
```

```
DIP SW  : straight == off
```

```
NetBtLd>
```

Swap the NBL flashes permanently

COMMAND / RESPONSE:

```
NetBtLd> swap -p
```

```
Flash config permanently swapped
```

```
NetBtLd
```



TFTP

FUNCTION:	Download file from a TFTP server
SYNTAX:	tftp [<serverip>] [<filename>] where: tftp command <serverip> parameter: string <nnn.nnn.nnn.nnn> IP address of the TFTP server <filename> parameter: string <x ... x> name of image file to be downloaded, or path and name of image file to be downloaded
DESCRIPTION:	The TFTP command makes it possible to download a file from a TFTP server via an Ethernet port. If used with the DHCP command, it is possible to use the IP address and file information returned by the DHCP command. If this command is issued without any parameters, it will use the previously stored information returned with the DHCP command.
USAGE:	Download a file from a TFTP server. COMMAND / RESPONSE (none): tftp 195.178.125.55 image2 This command downloads the file "image2" from the specified TFTP server.

VER

FUNCTION:	Display version number
SYNTAX:	ver
DESCRIPTION:	The command VER displays the actual version number of the NetBootLoader.



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Chapter

6

Power Considerations



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6. Power Considerations

6.1 AM4100 Voltage Ranges

The AM4100 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The AM4100 requires two power sources, the module management power for the MMC (nominal: 3.3V DC) and a single payload power (nominal: 12V DC) for the module components.

The following table specifies the ranges for the different input power voltages within which the board is functional. The AM4100 is not guaranteed to function if the board is not operated within the operating range.

Table 6-1: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	OPERATING RANGE
Payload Power (nominal: 12V DC)	10.0 V min. to 14.0 V max.	10.8 V min. to 13.2 V max.
Module Management Power (nominal: 3.3V DC)	2.97 V min. to 3.63 V. max. ($\pm 10\%$)	3.135 V min. to 3.465 V max. ($\pm 5\%$)



Warning!

The AM4100 must not be operated beyond the absolute range indicated in the table above. Failure to comply with the above may result in damage to the board.

6.2 Carrier Power Requirements

6.2.1 Payload Power

Payload power is the power provided to the module from the carrier or the backplane for the main function of the module. The payload power voltage should be selected at the higher end of the specified voltage range. The continuous current limit value is based on the power limit of 60 W per module at the minimum supply value. The maximum current value for the payload power is derived from a 25% derating of the connector pins, which allow a total of 6.0 A (0.75 A per pin; 8 pins).

The payload power voltage shall be at least 10.8 V and not more than 13.2 V at the module contacts during normal conditions under all loads (see Table 6-1, "DC Operational Input Voltage Ranges"). The bandwidth-limited periodic noise due to switching power supplies or any other source shall not exceed 200 mV peak to peak.



6.2.2 Payload and MMC Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the AM4100:

- Beginning at 10% of the nominal output voltage, the voltage must rise within $> 0.1 \text{ ms}$ to $< 20 \text{ ms}$ to the specified regulation range of the voltage. Typically: $> 5 \text{ ms}$ to $< 15 \text{ ms}$.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.

The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal V_{out} .

6.2.3 Module Management Power Consumption

The module management power is used only for the Module Management Controller (MMC), which has a very low power consumption. The management power voltage measured on the AMC at the connector shall be $3.3 \text{ V} \pm 5\%$ and the maximum current is 100 mA (see Table 6-1, "DC Operational Input Voltage Ranges").

6.3 Payload Power Consumption of the AM4100

The goal of this description is to provide a method to calculate the payload power consumption for the AM4100 board with different configurations and applications. The processor and the memory dissipate the majority of the payload power.

The payload power consumption tables below list the voltage and power specifications for the AM4100 board using Freescale™ MPC8641D dual-core PowerPC® processors and various memory sizes.

During the power measurements, the Linux OS with the NBench benchmark software was used providing 99% workload on both cores. All measurements were conducted at a temperature of 25°C with a nominal payload power of 12 V and with the following interfaces connected:

- Two front Gigabit Ethernet ports
- One front serial port

The module management power is below 0.3 W and it was therefore not considered for these measurements. The measured values varied, because the power consumption was dependent on processor activity.



Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the component variation.

The payload power consumption was measured using the following processors:

- Freescale MPC8641D processor, 1.0 GHz, 400 MHz platform frequency (MC8641DVU1000GB)
- Freescale MPC8641D processor, 1.32 GHz, 528 MHz platform frequency (MC8641DVU1333JB)
- Freescale MPC8641D processor, 1.5 GHz, 600 MHz platform frequency (MC8641DVU1500KB)

with the Linux operating system with the NBench benchmark software.



The following tables indicate the power consumption of the AM4100 with various processors frequencies and airflow conditions. The airflow has a direct influence on the CPU's die temperature and thus on the CPU's power consumption.

Table 6-2: Power Consumption: AM4100 MPC8641D, 1.0 GHz, 400 MHz Platform Freq.

AIRFLOW	3 m/s	2.5 m/s	2 m/s	1.5 m/s	1 m/s	0.6 m/s
POWER CONSUMPTION	28 W	29 W	30 W	30 W	31 W	33 W

Table 6-3: Power Consumption: AM4100 MPC8641D, 1.32 GHz, 528 MHz Platform Freq.

AIRFLOW	3 m/s	2.5 m/s	2 m/s	1.5 m/s	1 m/s	0.6 m/s
POWER CONSUMPTION	31 W	32 W	32 W	33 W	34 W	35 W

Table 6-4: Power Consumption: AM4100 MPC8641D, 1.5 GHz, 600 MHz Platform Freq.

AIRFLOW	3 m/s	2.5 m/s	2 m/s	1.5 m/s	1 m/s	0.6 m/s
POWER CONSUMPTION	40 W	40 W	42 W	43 W	47 W	50 W

6.4 IPMI FRU Payload Power Consumption

The following table indicates the IPMI FRU payload power consumption values stored in the E-Keying data.

Table 6-5: IPMI FRU Payload Power Consumption of the AM4100

MEMORY CONFIGURATION	MPC8641D 1.0 GHz	MPC8641D 1.32 GHz	MPC8641D 1.5 GHz
512 MB/1 GB /2 GB	3.1 A (37.2 W)	3.1 A (37.2 W)	4.6 A (55.2 W)

6.5 Payload Start-Up Current of the AM4100

The following tables indicate the payload start-up current of the AM4100 during the first 2-3 seconds after the payload power has been applied. The payload power consumption of the AM4100 during operation is indicated in Tables 6-2 to 6-4.

Table 6-6: Payload Start-Up Current of the AM4100

START-UP CURRENT	MPC8641D 1.0 GHz	MPC8641D 1.32 GHz	MPC8641D 1.5 GHz
peak	7.2 A	7.2 A	7.2 A
average	2.3 A	2.1 A	2.5 A

For further information on the start-up current, contact Kontron's Technical Support.



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Chapter

7

Thermal Considerations



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7. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing AM4100 applications.

7.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AM4100, all onboard components must remain within the maximum temperature specifications. The most critical components on the AM4100 are the processor and the memory. Operating the AM4100 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the Module Management Controller supports several temperature monitoring and control features.

The AM4100 includes five temperature sensors that are accessible via the Module Management Controller. They are distributed over the complete board to measure the onboard temperature values.

Although temperature sensing information is made available to the MMC, the AM4100 itself does not provide any active means of temperature regulation by default.

7.1.1 Placement of the Temperature Sensors

Figure 7-1: Processor Temperature Sensor Placement (AM4100 Top View)

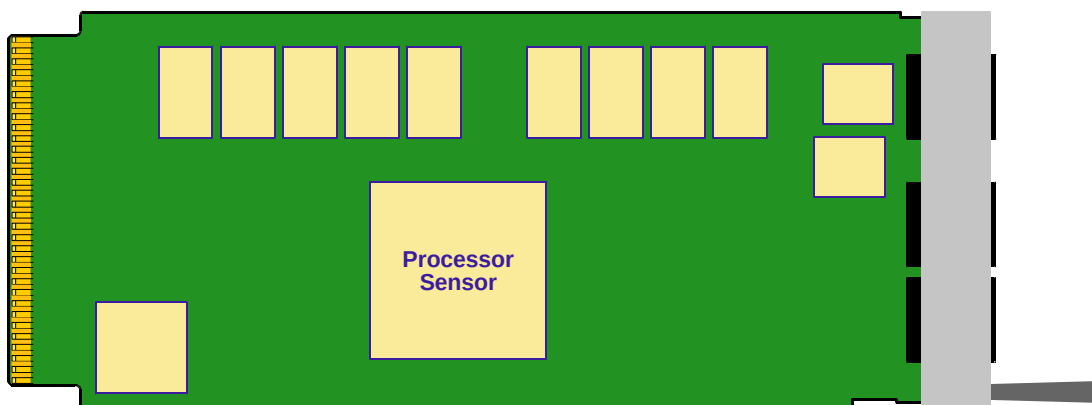
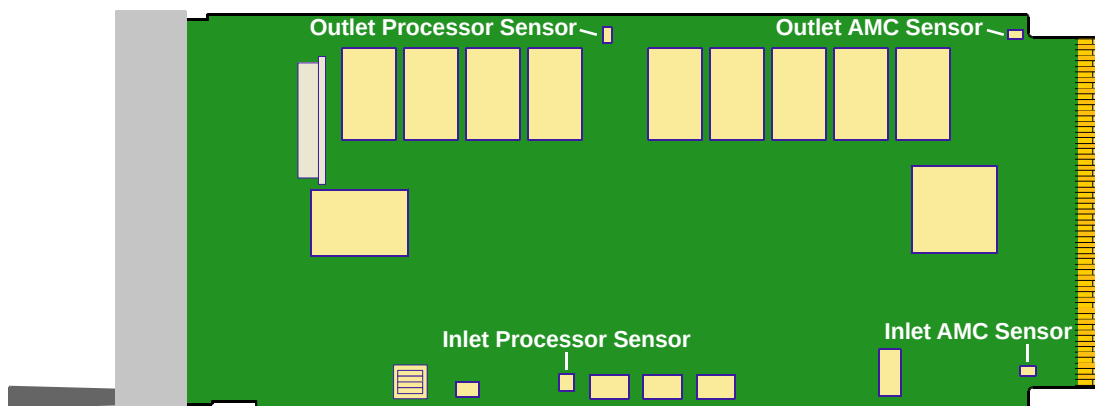


Figure 7-2: Board Temperature Sensor Placement (AM4100 Bottom View)





7.1.2 Board Thermal Monitoring

The AM4100 includes four board temperature sensors distributed over the complete board to measure the board temperature (see Figure 7-2). The board temperature sensors are accessible via the Module Management Controller.

The AM4100 uses the following board temperature sensors:

- Inlet board temperature sensor near the AMC Card-edge connector (Inlet AMC Sensor)
- Outlet board temperature sensor near the AMC Card-edge connector (Outlet AMC Sensor)
- Inlet board temperature sensor near the processor (Inlet Processor Sensor)
- Outlet board temperature sensor near the processor (Outlet Processor Sensor)

7.1.3 Processor Thermal Monitoring

The Freescale MPC8641D processor includes one die temperature sensor (Processor Sensor), as illustrated in Figure 7-1.

Via the Processor Sensor, the Module Management Controller can measure the processor die temperature.

The maximum die temperatures for all processor types is as follows:

- Freescale MPC8641D: all versions: 105 °C

7.2 CPU Internal Thermal Regulation

The Instruction Cache Throttling mechanism allows for the reduction of the CPU's power consumption and thus the CPU's temperature. This mechanism requires a dedicated software such as a thermal management application or an OS daemon. For further information about the Instruction Cache Throttling, refer to the MPC8641D Integrated Host Processor Family Reference Manual.

7.3 External Thermal Regulation

The external thermal regulation of the AM4100 is realized using a dedicated heat sink in conjunction with a system chassis that provides thermal supervision, controlled system airflow and thermal protection, such as increased airflow, reduced ambient air temperature, or power removal.

The heat sink provided on the AM4100 has been specifically designed to ensure the best possible basis for operational stability and long-term reliability. The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, it has been specifically designed to efficiently support forced airflow concepts as found in modern AMC carriers and MicroTCA systems.



7.3.1 Forced Airflow

When developing applications using the AM4100, the system integrator must be aware of the overall system thermal requirements. System chassis must be provided which satisfy these requirements. As an aid to the system integrator, characteristics graphs are provided for the AM4100.



Warning!

As Kontron assumes no responsibility for any damage to the AM4100 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the AM4100 complies with the thermal considerations set forth in this document.

7.3.2 Thermal Characteristic Graphs

The thermal characteristic graphs shown on the following pages illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version is provided. When operating below the indicated curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the indicated curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance, if implemented, or finally in an emergency stop in order to protect the CPU from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, a safe operation is guaranteed. Above this operating point, the chassis thermal management must become active and take the necessary steps to protect the CPU from thermal destruction.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in m³/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m³/h; 1 m³/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s = meter-per-second or in fps = feet-per-second, respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps



The following figures illustrate the operational limits of the AM4100 taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made using a Kontron AMC test system and the Nbench benchmark software running under Linux. Both processor cores were enabled during the measurements.

**Note ...**

The maximum airflow input temperature was measured at the bottom of the board just before the air flowed over the board.

**Warning!**

In all situations, the maximum case temperature of the processors must be kept below the maximum allowable temperature.

Figure 7-3: Operational Limits for the Mid-Size AM4100 with 1.0 GHz

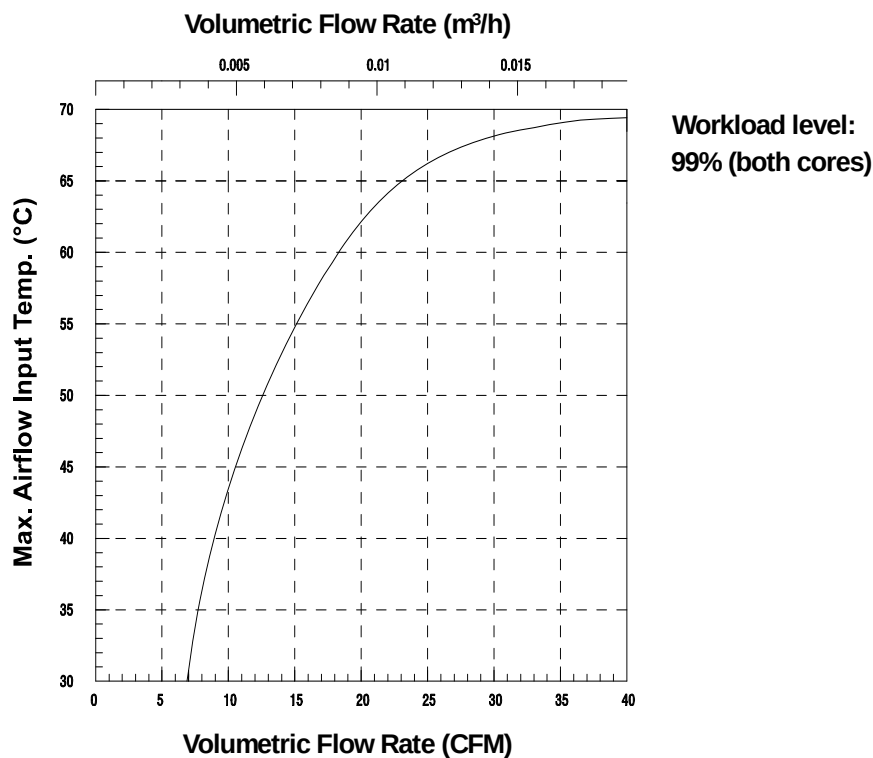




Figure 7-4: Operational Limits for the Mid-Size AM4100 with 1.32 GHz

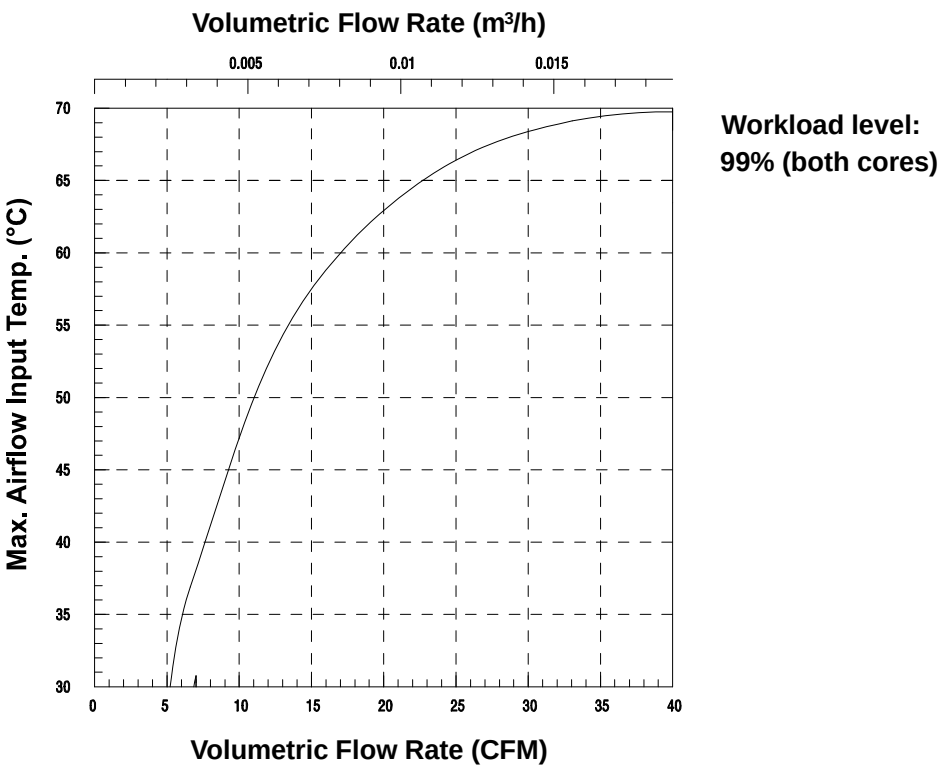
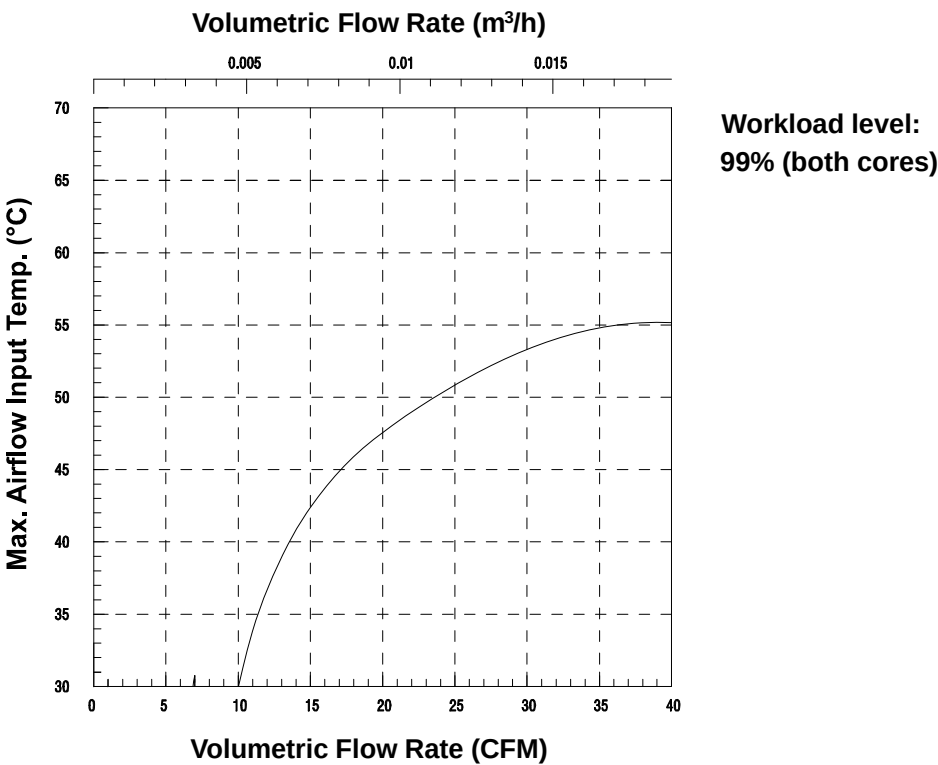


Figure 7-5: Operational Limits for the Full-Size AM4100 with 1.5 GHz

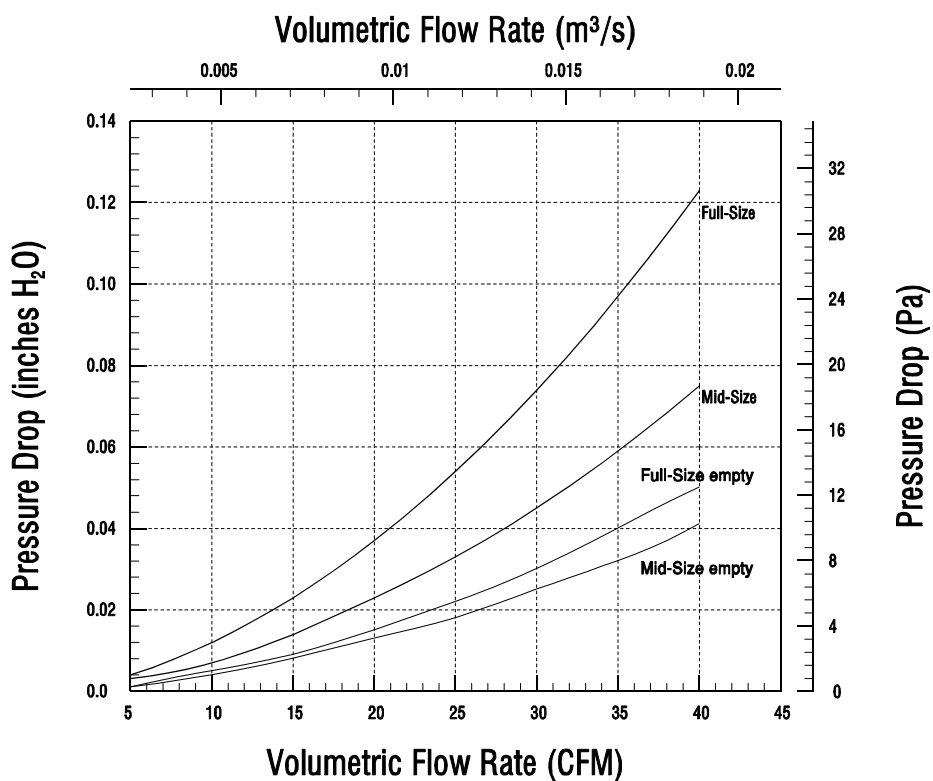


7.3.3 Airflow Impedance

In order to determine the cooling requirements of the AM4100, the airflow impedance of a Mid-size and a Full-size AM4100 module has been determined via simulation. No card guides or struts have been used for the simulations because the resulting airflow impedance depends on individual configuration of the AMC carrier or MicroTCA system.

The following figure shows the impedance curves of a Mid-size and a Full-size AM4100 module.

Figure 7-6: Mid-Size and Full-Size AM4100 Impedance Curves



The following table indicates the pressure drop at 10, 20, 30, and 40 CFM volumetric flow rates.

Table 7-1: Pressure Drop vs. Airflow Data

VOLUMETRIC FLOW RATE [CFM]	PRESSURE DROP [inches H ₂ O]			
	MID-SIZE	MID-SIZE EMPTY	FULL-SIZE	FULL-SIZE EMPTY
10	0.007	0.004	0.012	0.005
20	0.023	0.013	0.037	0.015
30	0.045	0.025	0.074	0.030
40	0.075	0.041	0.123	0.050

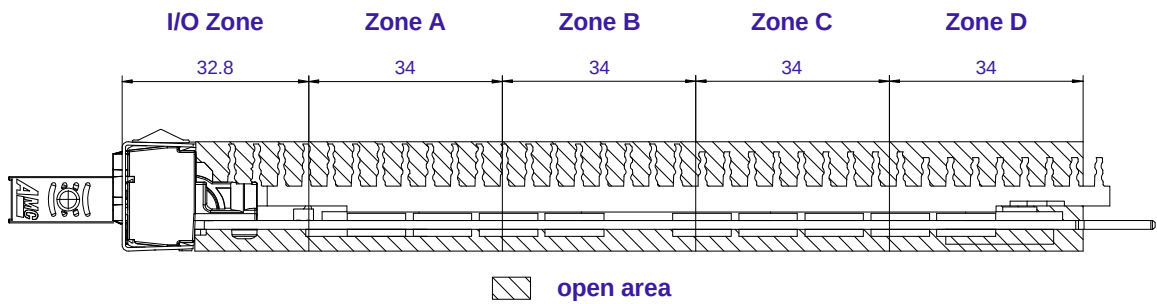


7.3.4 Airflow Paths

The area between the front panel and the AMC Card-edge connector is divided into five zones, one I/O zone and four uniform thermal zones, A, B, C, and D. The PICMG AMC.0 Specification states that the uniformity of the airflow paths' resistance should provide an impedance on the A, B, C, and D zones that is within $\pm 25\%$ of the average value of the four thermal zones.

The following figure shows the thermal zones of a Mid-size AM4100.

Figure 7-7: Thermal Zones of the Mid-Size AM4100 Module



The following table indicates the deviation of the airflow rate on a Mid-size AM4100 module.

Table 7-2: Deviation of the Airflow Rate on a Mid-Size AM4100

VOLUMETRIC FLOW RATE [CFM]	DEVIATION OF THE AIRFLOW RATE			
	ZONE A	ZONE B	ZONE C	ZONE D
10	-0.58%	-0.58%	1.73%	-0.58%
20	0.00%	0.00%	1.16%	-1.16%
30	0.00%	0.00%	1.16%	-1.16%
40	0.00%	0.00%	1.16%	-1.16%



Note ...

The Mid-size AM4100 module has an airflow rate deviation of max. $\pm 1.8\%$ of the average value of the four thermal zones (max. $\pm 25\%$ is allowed).
Positive deviation means increased airflow.
Negative deviation means decreased airflow.



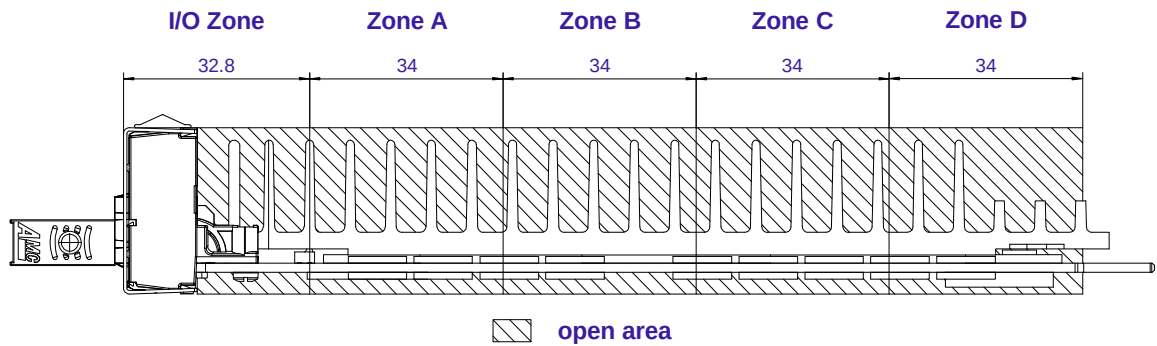
Note ...

The Mid-size AM4100 module provides an open area of 43%. According to the PICMG AMC.0 Specification, an open area of 20 to 70% perpendicular to the airflow path is recommended.



The following figure shows the thermal zones of a Full-size AM4100.

Figure 7-8: Thermal Zones of the Full-Size AM4100 Module



The following table indicates the deviation of the airflow rate on a Full-size AM4100 module.

Table 7-3: Deviation of the Airflow Rate on a Full-Size AM4100

VOLUMETRIC FLOW RATE [CFM]	DEVIATION OF THE AIRFLOW RATE			
	ZONE A	ZONE B	ZONE C	ZONE D
10	2.83%	0.43%	-1.98%	-1.29%
20	2.58%	0.29%	-1.43%	-1.43%
30	2.87%	0.57%	-1.72%	-1.72%
40	2.80%	0.50%	-1.51%	-1.79%



Note ...

The Full-size AM4100 module has an airflow rate deviation of max. $\pm 1.8\%$ of the average value of the four thermal zones (max. $\pm 25\%$ is allowed).

Positive deviation means increased airflow.

Negative deviation means decreased airflow.



Note ...

The Full-size AM4100 module provides an open area of 56%. According to the PICMG AMC.0 Specification, an open area of 20 to 70% perpendicular to the airflow path is recommended.

